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Krishna (MS-7647)

UATX Version: 0A

CPU: Intel Core 2 Quad (York field & Kentsfield),
Core 2 Duo (Wolfdale),Conroe-1333/1066/800MHz,
Pentium Dual core, Celeron Dual core
and Celeron-L series processors

System Chipset:

Intel Eaglelake - G43 (North Bridge)
Intel ICH10 (South Bridge)

On Board Device:

CLOCK Gen -- SILEGO SLG8XP51
LPC Super I/O -- Winbond 83667HG-B
LAN -- Realtek 8111DL (PCIE)
HD Audio Codec -- ALC888S-VC2

Main Memory:

Dual-channel DDR-III * 4

Expansion Slots:

PCI EXPRESS X16 SLOT *1
PCI EXPRESS X1 SLOT * 2
PCI SLOT * 1

PWM: ISL6334 4Phase

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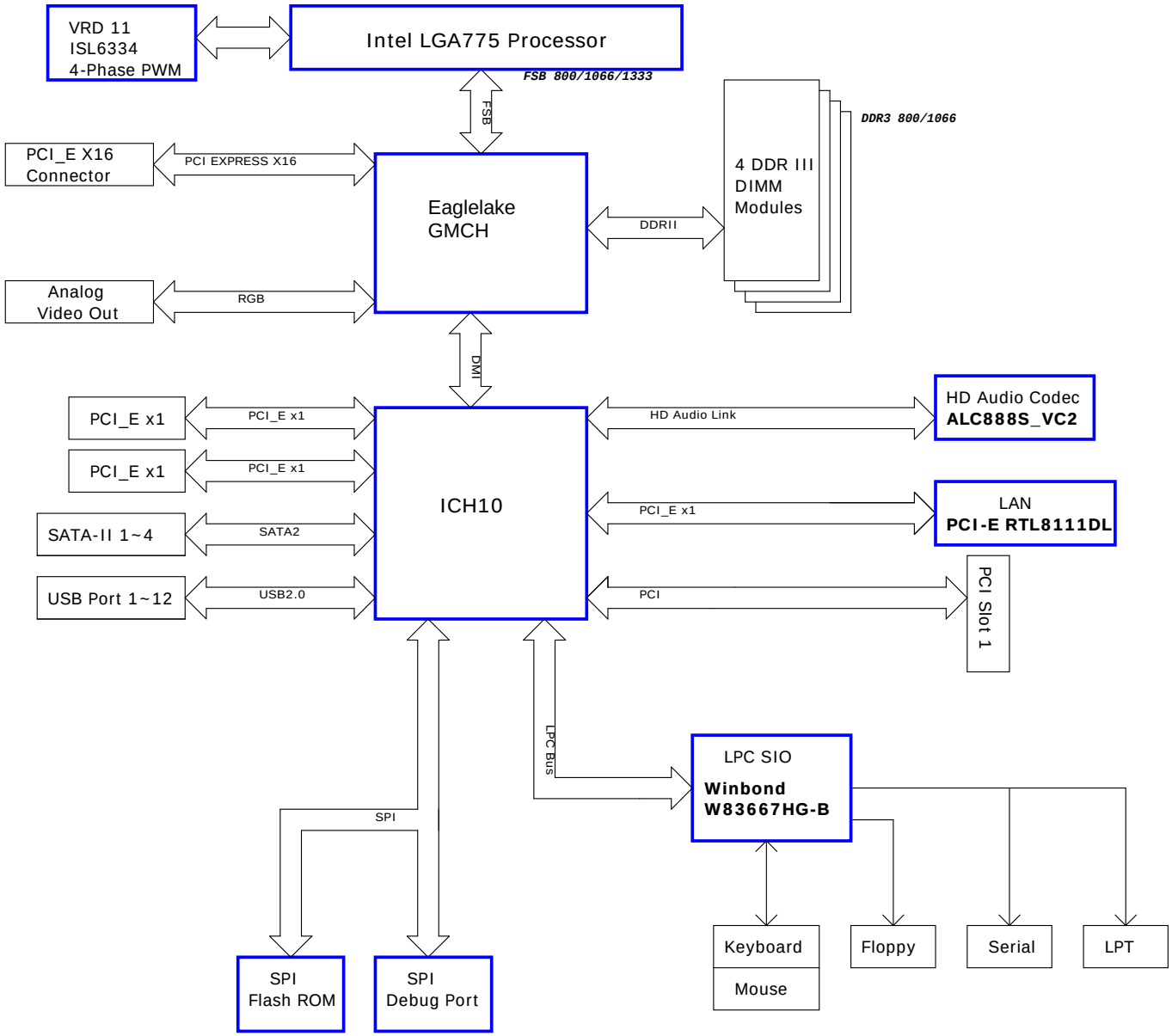
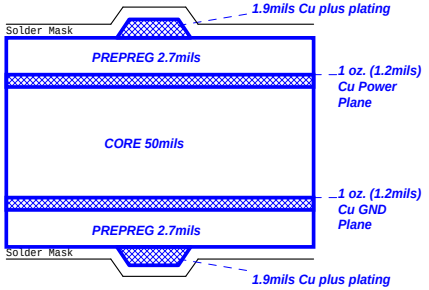
Block Diagram



Board Stack-up

(1080 Prepreg Considerations)



Single End 50ohm Top/Bottom : 4mils
USB2.0 - 90ohm : 15/4.5/7.5/4.5/15
SATA - 95ohm : 15/4/8/4/15
LAN - 100ohm : 15/4/8/4/15
PCIE - 95ohm : 15/4/8/4/15

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0A change to 0B

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	Krishna (MS-7647)	
Size: C	Document Description: Change history	Rev: 0A
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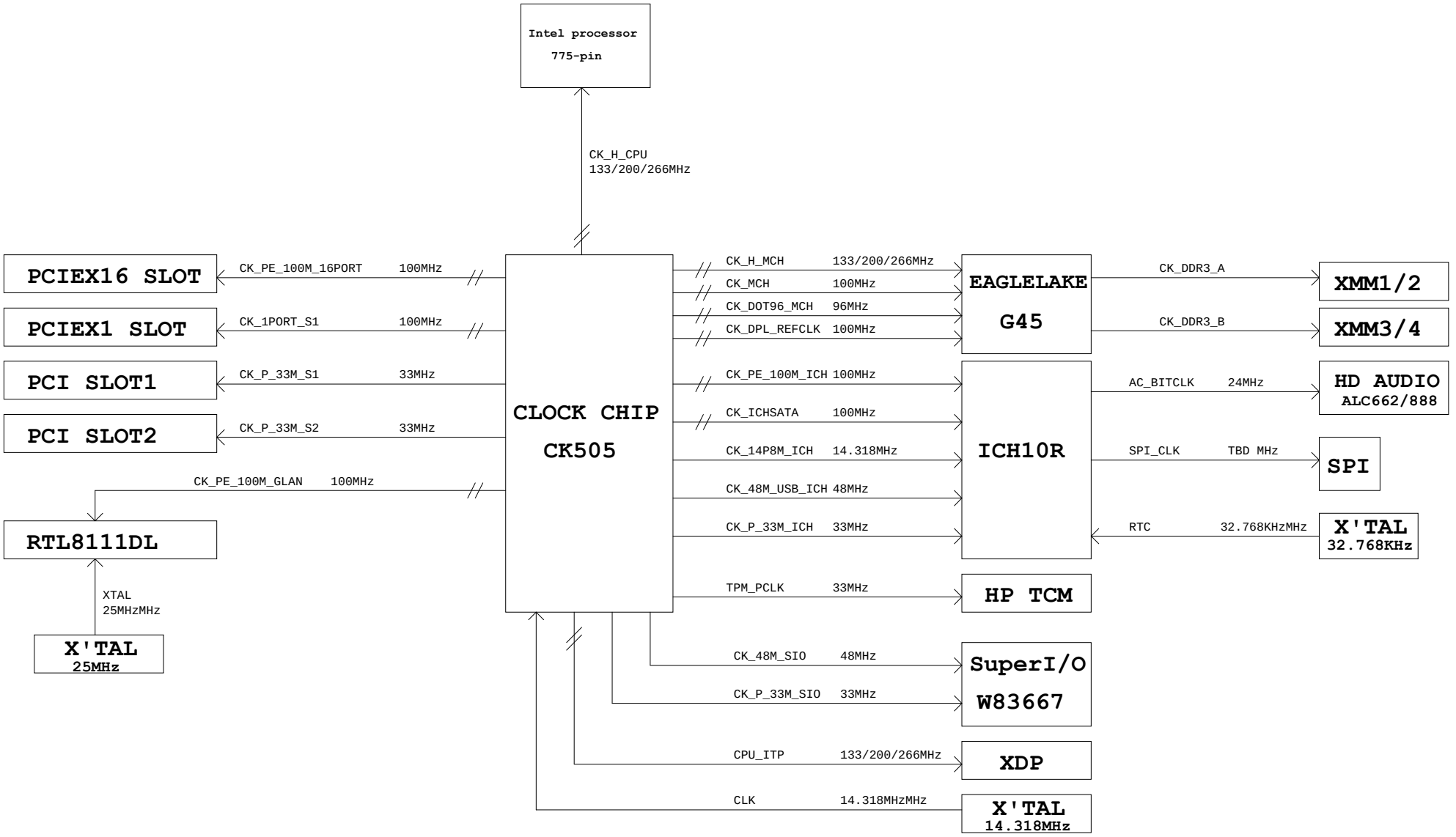

MSI	MICRO-STAR INT'L CO.,LTD	
	Krishna (MS-7647)	
Size: C	Document Description: Clock distribution	Rev: 0A
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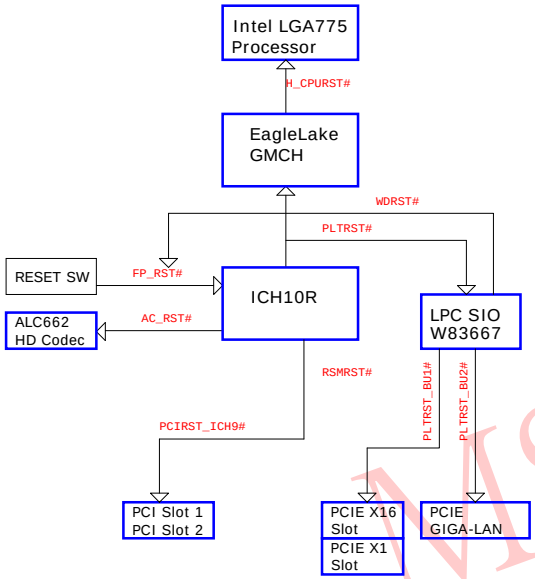
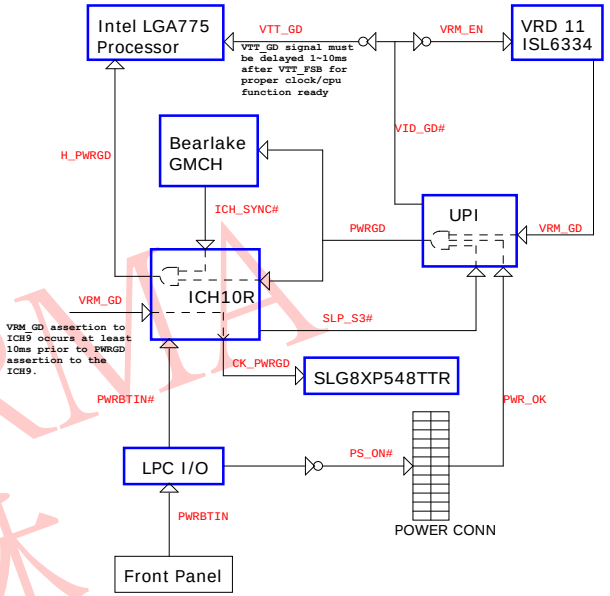
RESET MAP



PWROK MAP



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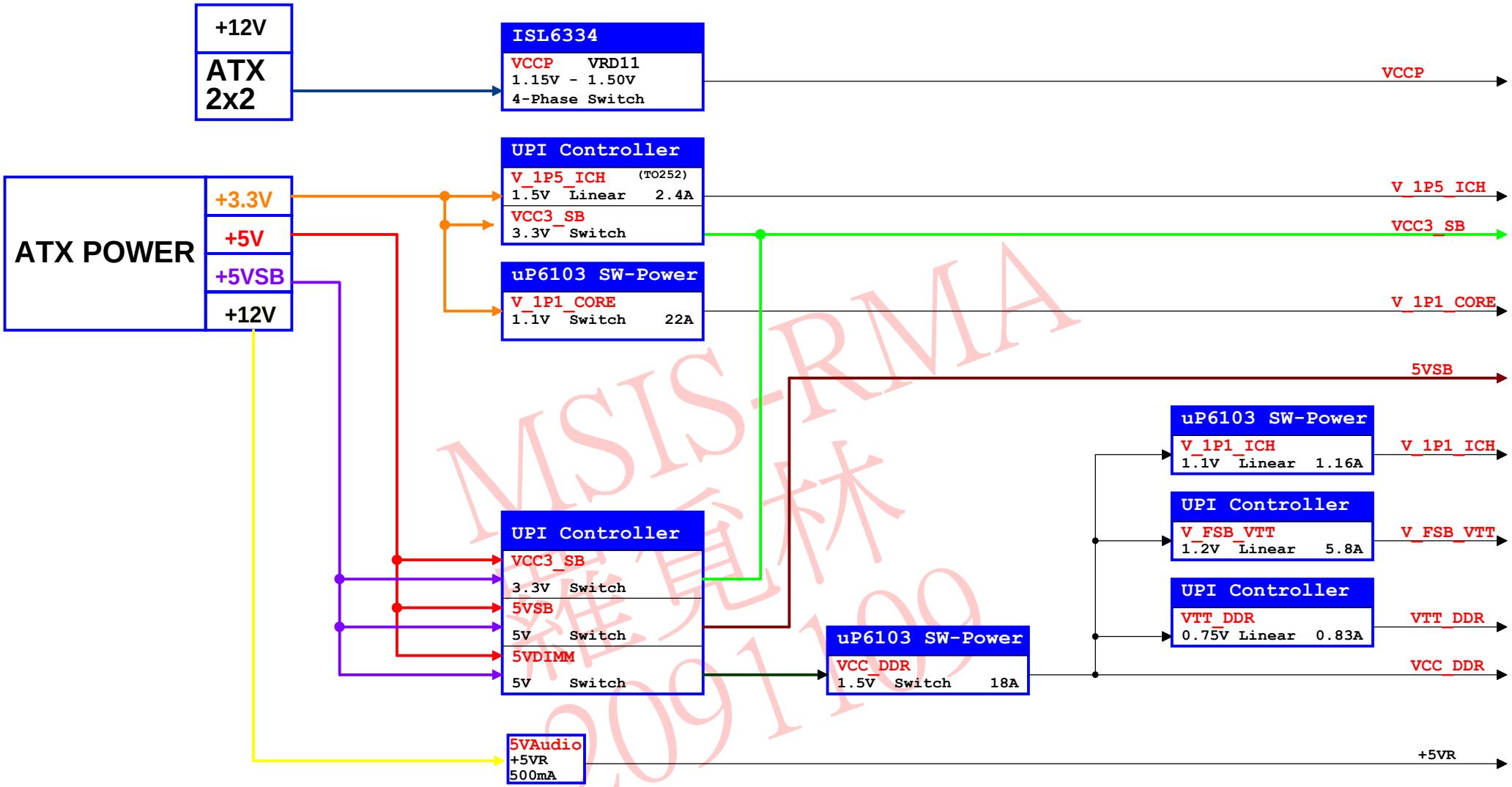
Krishna (MS-7647)

Size: Custom | Document Description: Signal & Reset Map | Rev: 0A

Date: Monday, October 19, 2009 | Sheet 5 of 38



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Size	Document Description	Rev
Custom	Power flow	0A

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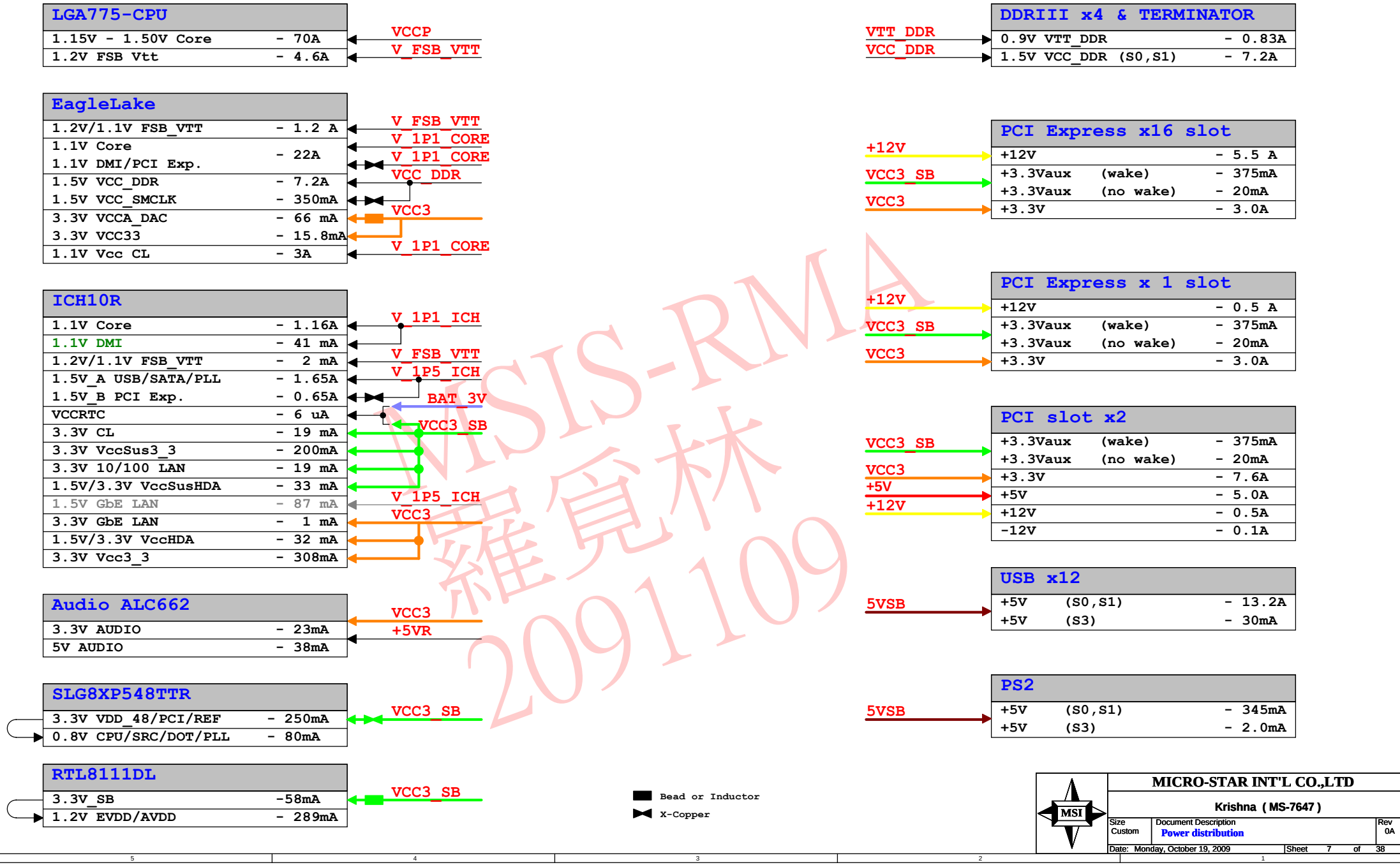

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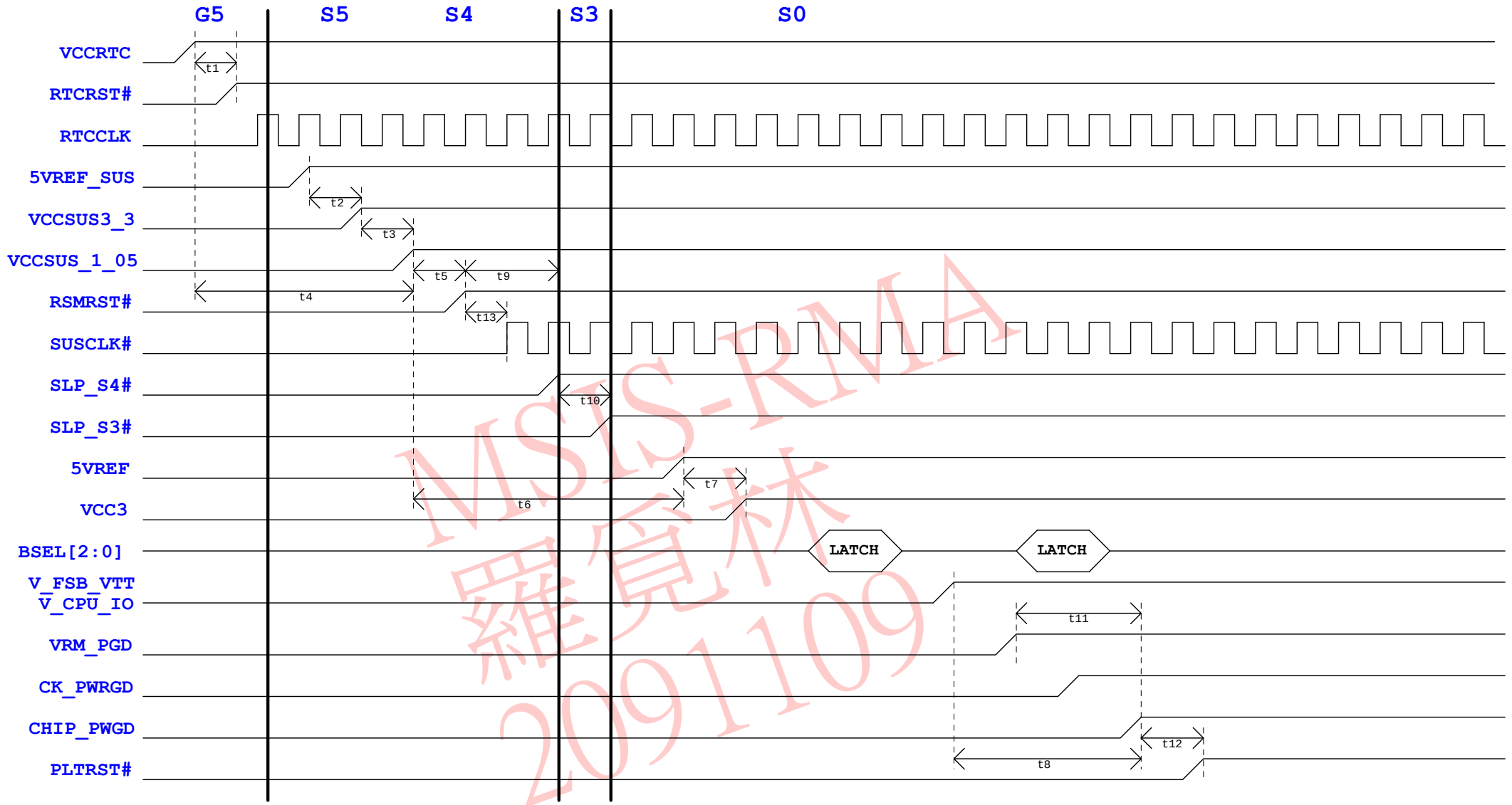

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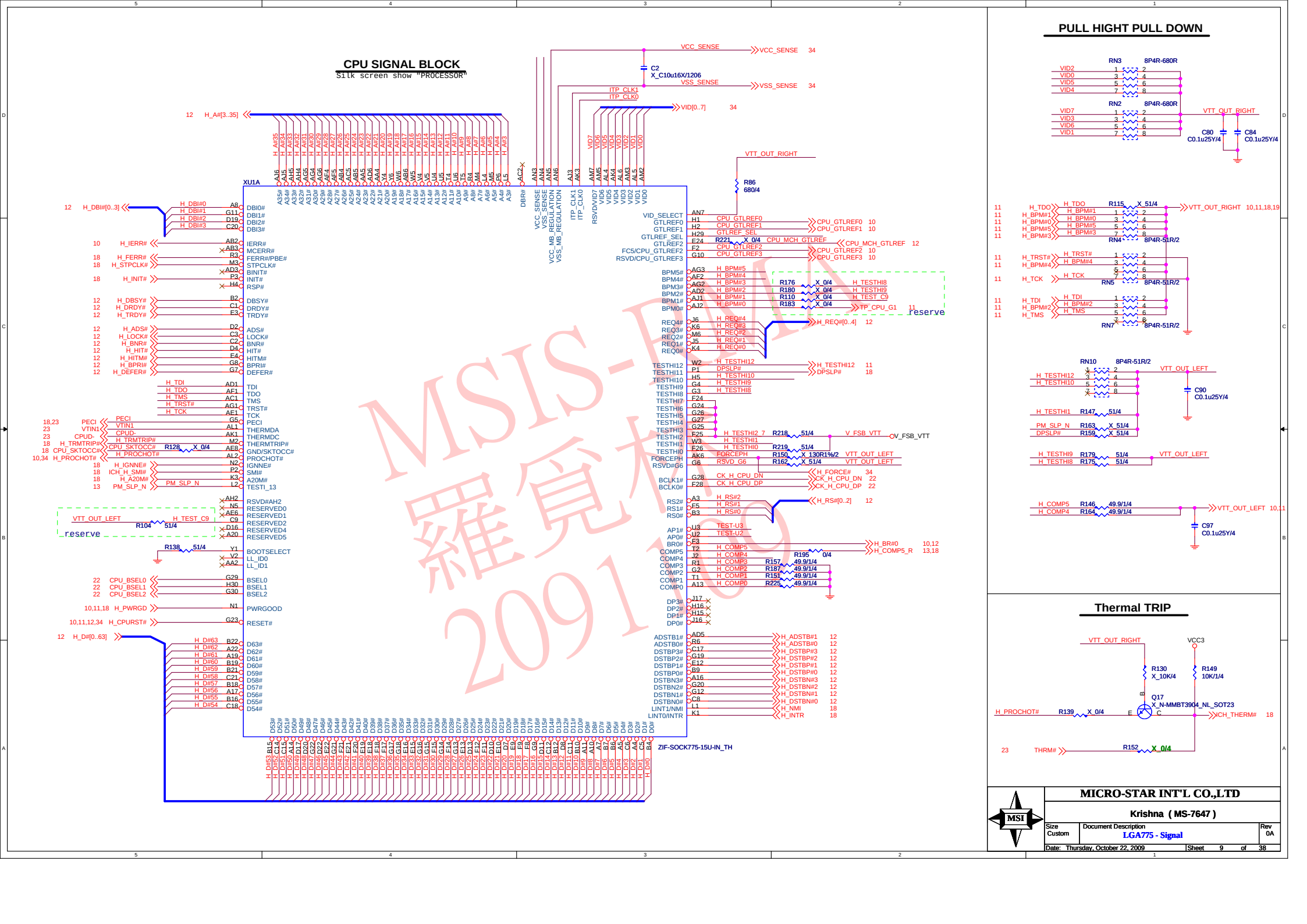
t1>18ms
t2>0ms
t3=0ms
t4>0ms
t5>10ms

t6>0ms
t7>0ms
t8>99ms
t9<110ms

t10>1RTCCLK
t11>5ms
t12:35~74RTCCLK
t13<110ms

MICRO-STAR INT'L CO.,LTD		
Krishna (MS-7647)		
Size: B	Document Description: Power sequence	Rev: 0A
Date: Monday, October 19, 2009	Sheet 8 of 38	


CPU SIGNAL BLOCK
Silk screen show "PROCESSOR"
XU1A
ZIF-SOCK775-15U-IN_TH
PULL HIGHT PULL DOWN
Thermal TRIP
MICRO-STAR INT'L CO.,LTD
Krishna (MS-7647)
LGA775 - Signal
Size Custom
Rev 0A
Date: Thursday, October 22, 2009
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MSIS-Hsin
羅宜君
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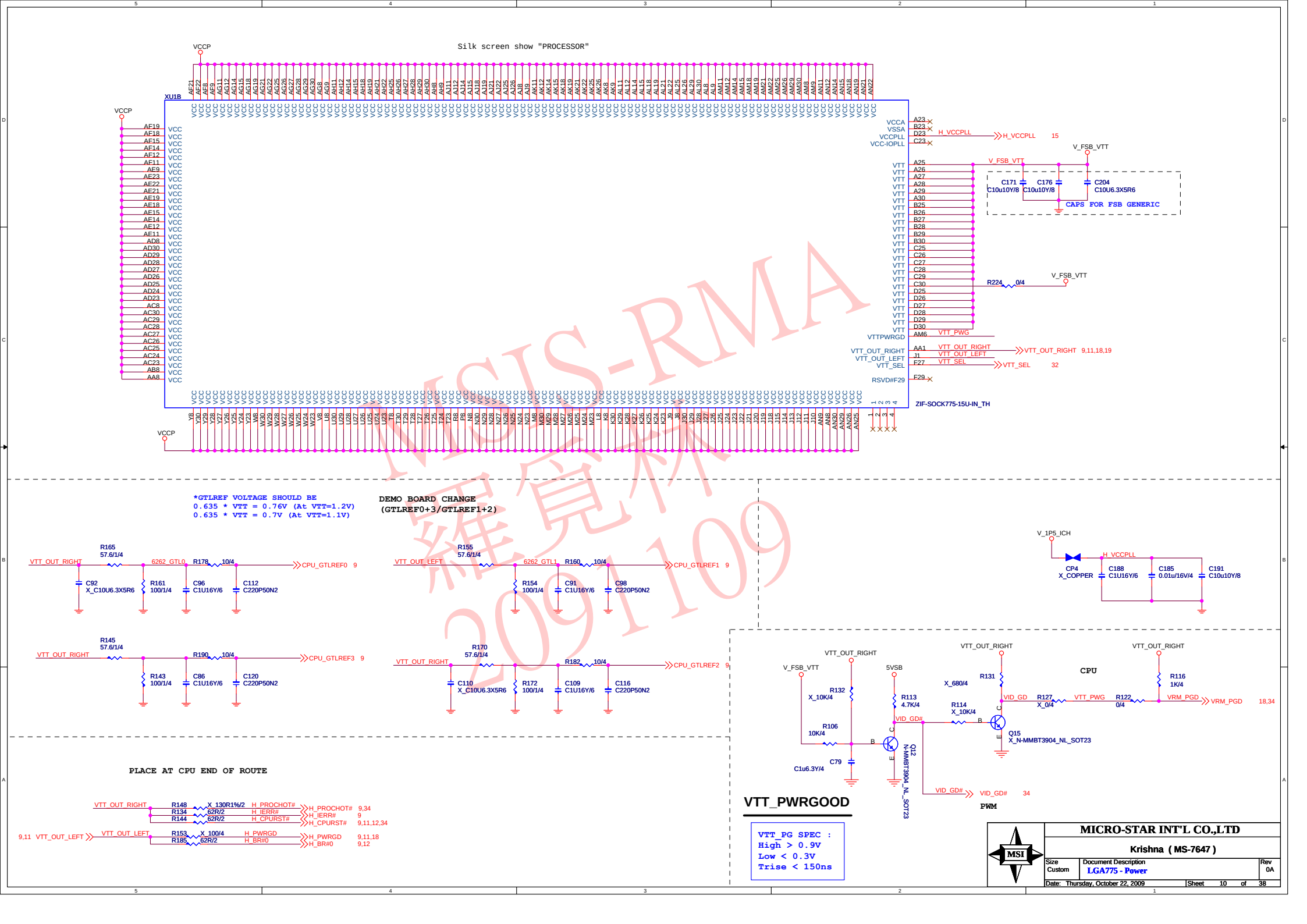
Silk screen show "PROCESSOR"
XU1B
ZIF-SOCK775-15U-IN_TH
CAPS FOR FSB GENERIC
*GTLREF VOLTAGE SHOULD BE
0.635 * VTT = 0.76V (At VTT=1.2V)
0.635 * VTT = 0.7V (At VTT=1.1V)
DEMO BOARD CHANGE
(GTLREF0+3/GTLREF1+2)
PLACE AT CPU END OF ROUTE
VTT_PWRGOOD
VTT_PG SPEC :
High > 0.9V
Low < 0.3V
Trise < 150ns
CPU
PWM
MICRO-STAR INT'L CO.,LTD
Krishna (MS-7647)
LGA775 - Power
Date: Thursday, October 22, 2009
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Silk screen show "PROCESSOR"

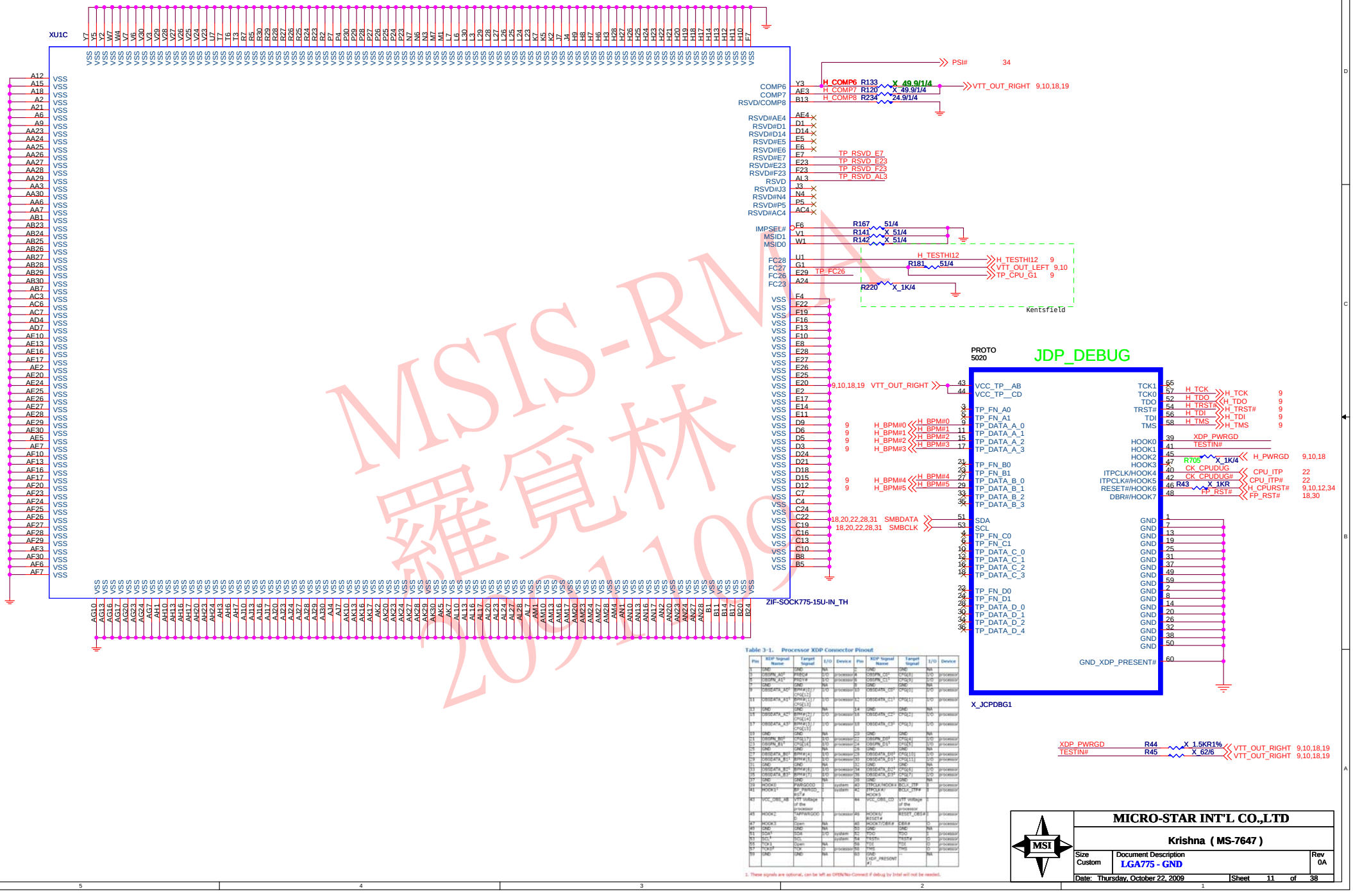

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Table 3-1. Processor XDP Connector Pinout

Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	GND	GND	NA		2	GND	GND	NA	
3	OBSFN_A0*	FERR#	I/O	processor	4	OBSFN_C0*	CFG[8]	I/O	processor
5	OBSFN_A1*	PECI#	I/O	processor	6	OBSFN_C1*	CFG[9]	I/O	processor
7	GND	GND	NA		8	GND	GND	NA	
9	OBSDATA_A0*	BPM#[0] / CFG[12]	I/O	processor	10	OBSDATA_C0*	CFG[0]	I/O	processor
11	OBSDATA_A1*	BPM#[1] / CFG[13]	I/O	processor	12	OBSDATA_C1*	CFG[1]	I/O	processor
13	GND	GND	NA		14	GND	GND	NA	
15	OBSDATA_A2*	BPM#[2] / CFG[14]	I/O	processor	16	OBSDATA_C2*	CFG[2]	I/O	processor
17	OBSDATA_A3*	BPM#[3] / CFG[15]	I/O	processor	18	OBSDATA_C3*	CFG[3]	I/O	processor
19	GND	GND	NA		20	GND	GND	NA	
21	OBSFN_B0*	CFG[17]	I/O	processor	22	OBSFN_D0*	CFG[4]	I/O	processor
23	OBSFN_B1*	CFG[18]	I/O	processor	24	OBSFN_D1*	CFG[5]	I/O	processor
25	GND	GND	NA		26	GND	NA		
27	OBSDATA_B0*	BPM#[4]	I/O	processor	28	OBSDATA_D0*	CFG[10]	I/O	processor
29	OBSDATA_B1*	BPM#[5]	I/O	processor	30	OBSDATA_D1*	CFG[11]	I/O	processor
31	GND	GND	NA		32	GND	GND	NA	
33	OBSDATA_B2*	BPM#[6]	I/O	processor	34	OBSDATA_D2*	CFG[6]	I/O	processor
35	OBSDATA_B3*	BPM#[7]	I/O	processor	36	OBSDATA_D3*	CFG[7]	I/O	processor
37	GND	GND	NA		38	GND	GND	NA	
39	HOOK0	PWRGOOD	I	system	40	TCLK/HOOK4	BCLK_ITP	I	processor
41	HOOK1	BF_PWRGD_L RST#	O	system	42	ITPCLK#/ HOOK5	BCLK_ITP#	I	processor
43	VCC_OBS_AB	VTT Voltage of the processor	I		44	VCC_OBS_CD	VTT Voltage of the processor	I	
45	HOOK2	THRMTRIP#	O	processor	46	HOOK6/ RESET#_OBS#2	RESET_OBS#2	O	processor
47	HOOK3	GND	NA		48	HOOK7/ OBS#3	OBS#3	IO	processor
49	GND	GND	NA		50	GND	GND	NA	
51	SDA*	SDA	I/O	system	52	TDO	TDO	O	processor
53	SCL*	SCL	I	system	54	TRST#	TRST#	I	processor
55	TCK1	Open	NA		56	TDI	TDI	I	processor
57	TCK0*	TCK	I	processor	58	TMS	TMS	I	processor
59	GND	GND	NA		60	GND (XDP_PRESENT#)	-	NA	

1. These signals are optional, can be left as OPEN/No-Connect if debug by Intel will not be needed.

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Size: Custom	Document Description: LGA775 - GND	Rev: 0A
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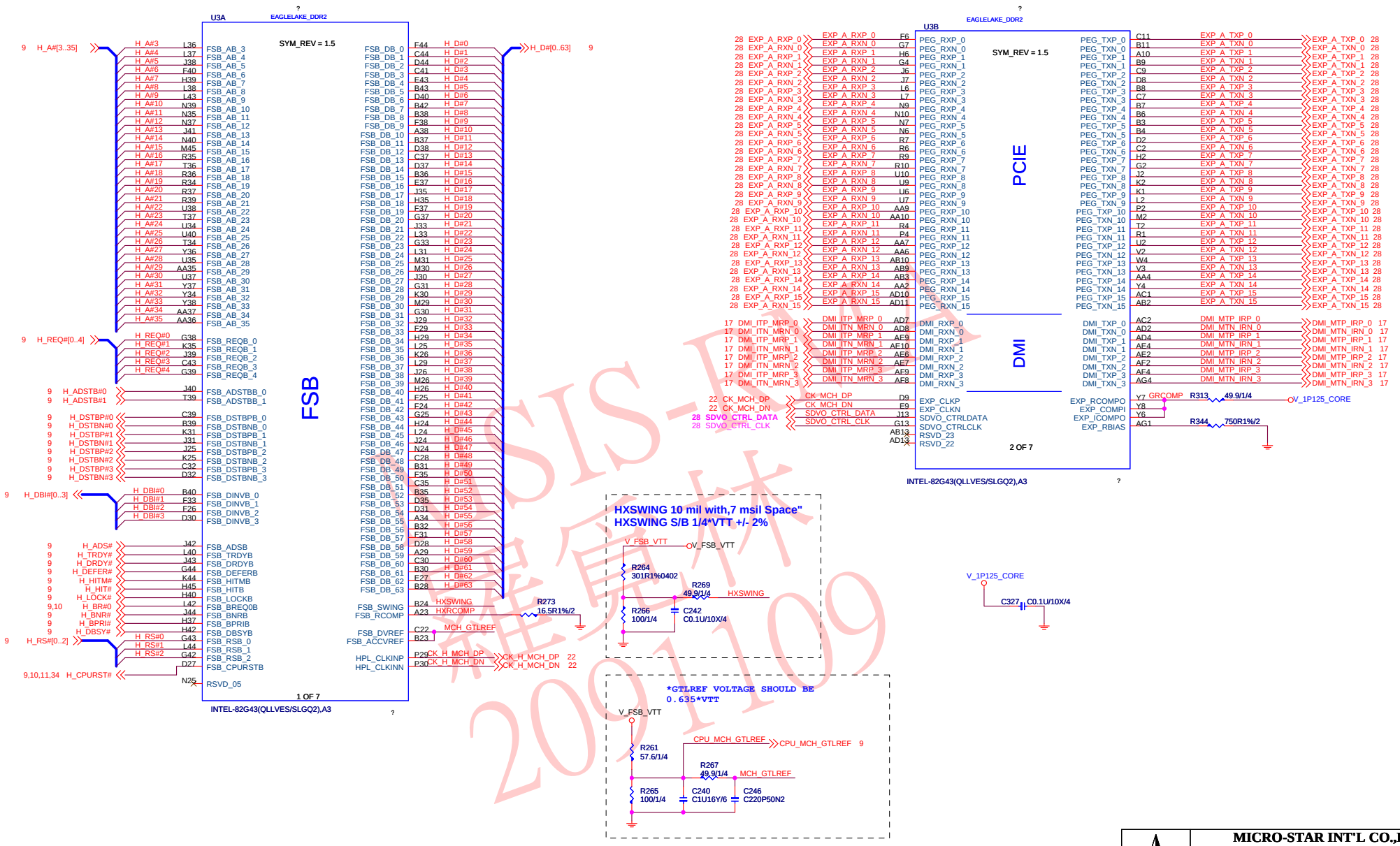
U3A
EAGLELAKE_DDR2
SYM_REV = 1.5
FSB
1 OF 7
INTEL-82G43(QLLVES/SLGQ2),A3
U3B
PCIE
DMI
2 OF 7
INTEL-82G43(QLLVES/SLGQ2),A3
HXSWING 10 mil with,7 msil Space"
HXSWING S/B 1/4*VTT +/- 2%
*GTLREF VOLTAGE SHOULD BE
0.635*VTT
MICRO-STAR INT'L CO.,LTD
Krishna (MS-7647)
Intel Eaglelake - FSB, PCIE, DMI
Date: Thursday, October 22, 2009
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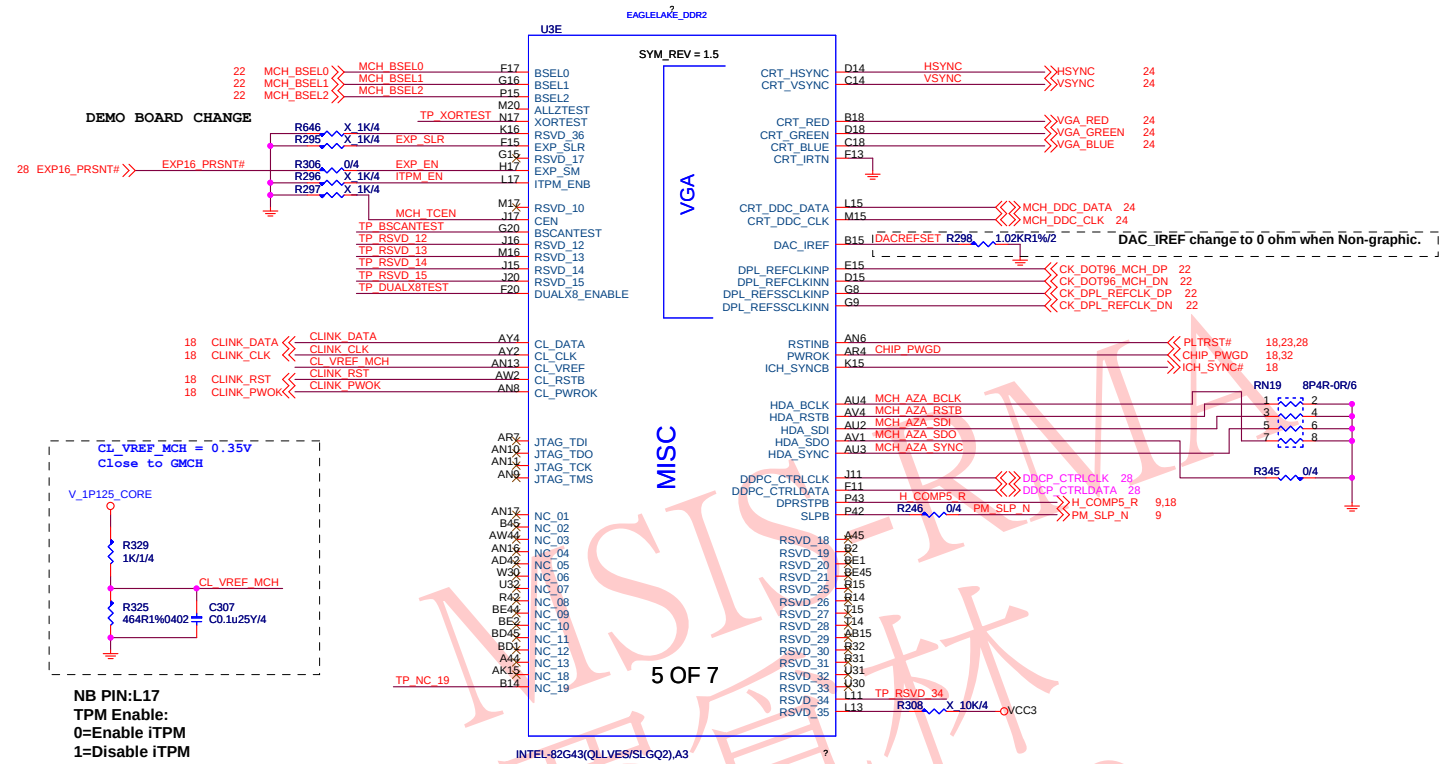

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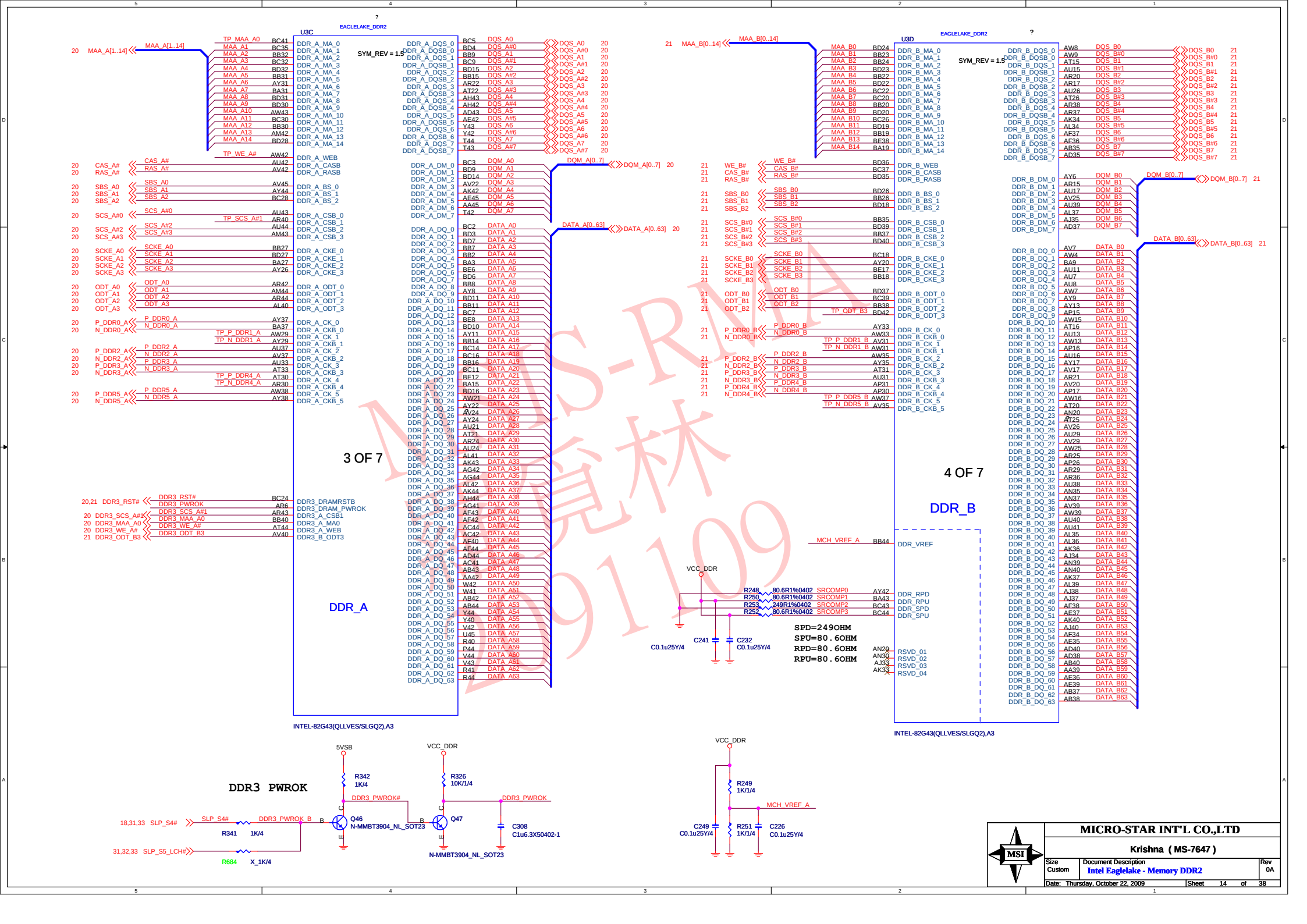
Size: Custom	Document Description: Intel Eaglelake - VGA, MSIC
Rev: 0A	
Date: Thursday, October 22, 2009	Sheet 13 of 38



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Krishna (MS-7647)	
Size: Custom	Document Description: Intel Eaglelake - Memory DDR2
Rev: 0A	
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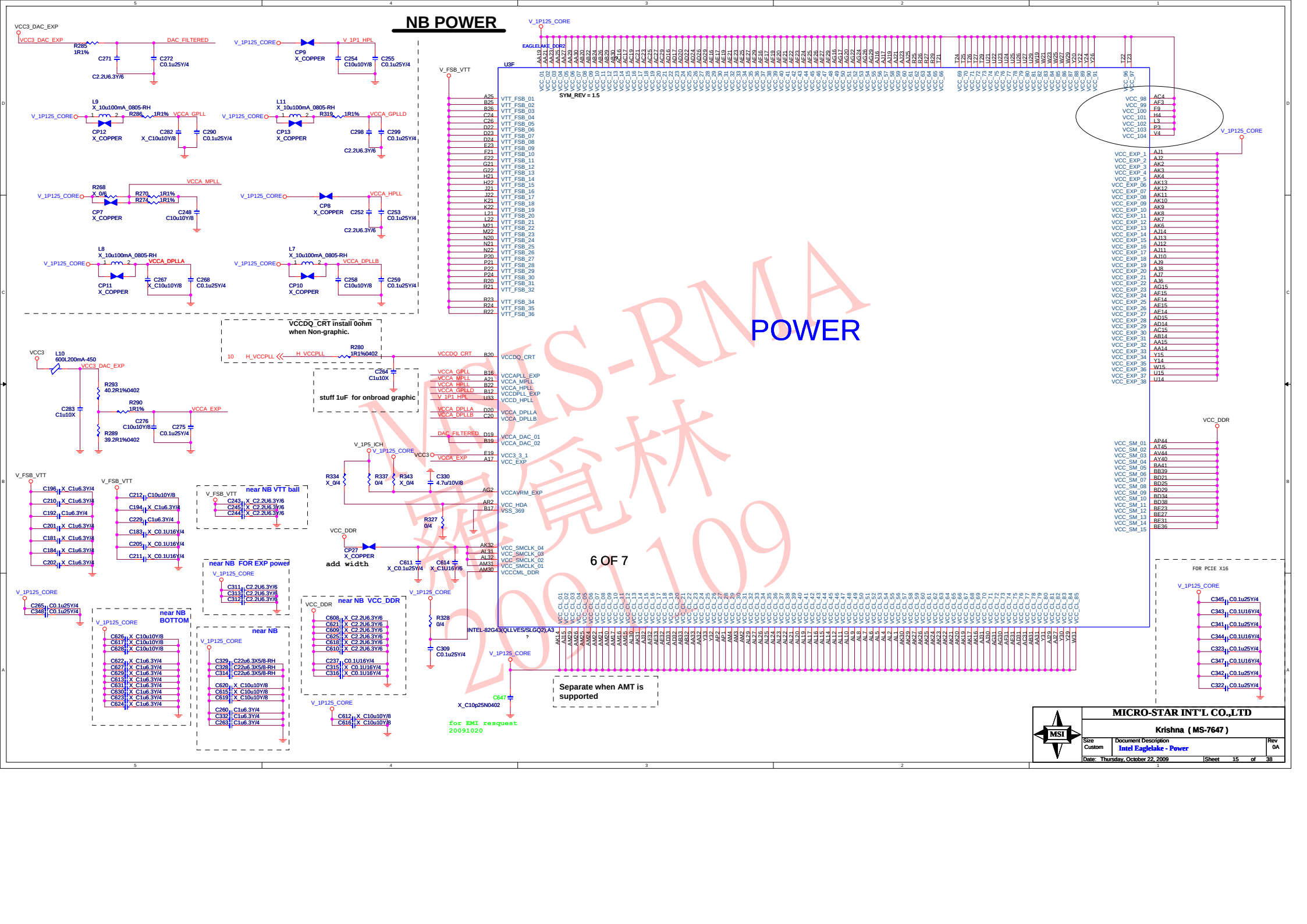
NB POWER



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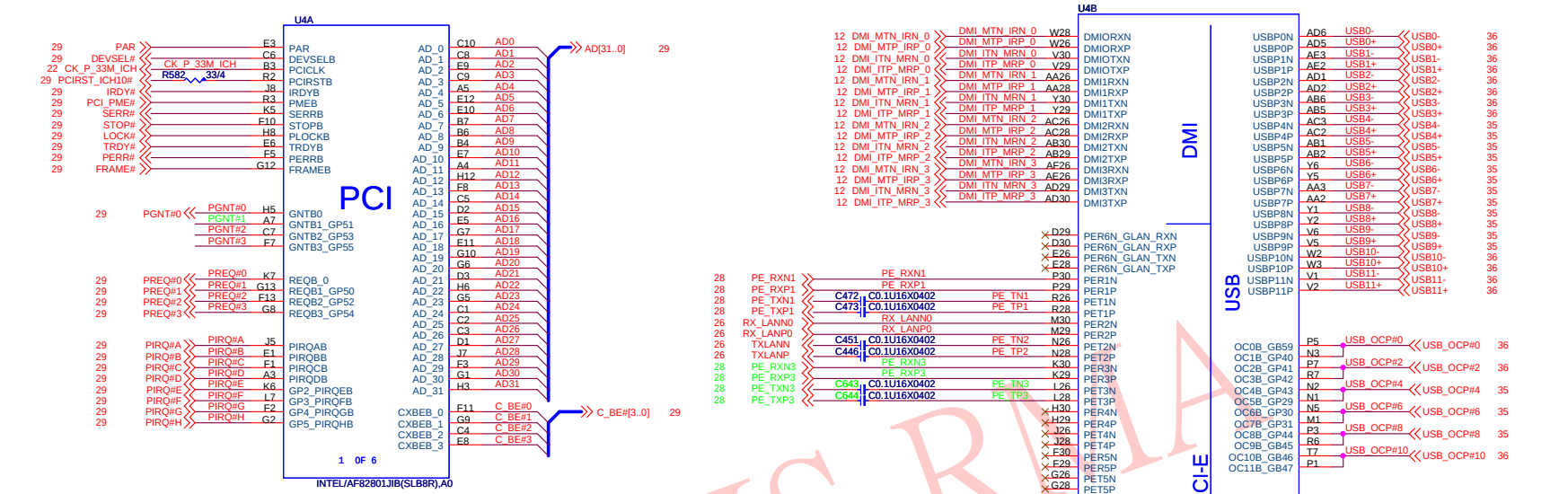
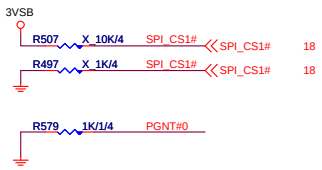
Krishna (MS-7647)			
Size: Custom	Document Description: Intel Eaglelake - GND		Rev: 0A
Date: Thursday, October 22, 2009	Sheet 16 of 38		



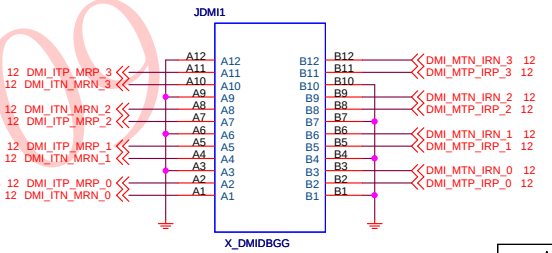


BOOT SELECT STRAPS		
BOOT DEVICE	GNT#0	SPI_CS1#
FWH	1	1
SPI	0	1
PCI	1	0

PGNT#[3:0]Internal Pull-up

SIGNAL	H	L	DES.
GNT3	DIS	EN	A16 OVERIDE
GNT2	N/A	SET BIT	PCIE PORT CONFIG 2 BIT 0 (5-6)

HDA_SDOUT/HDA_SYNC strap PCI_E port configuration bit[1:0].Internal weak pull down.
00:1X/1X/1X/1X 11:0X/0X/4X



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Size	Document Description	Rev
Custom	ICH10R - PCI, DMI, USB, PCIE & Slots	0A
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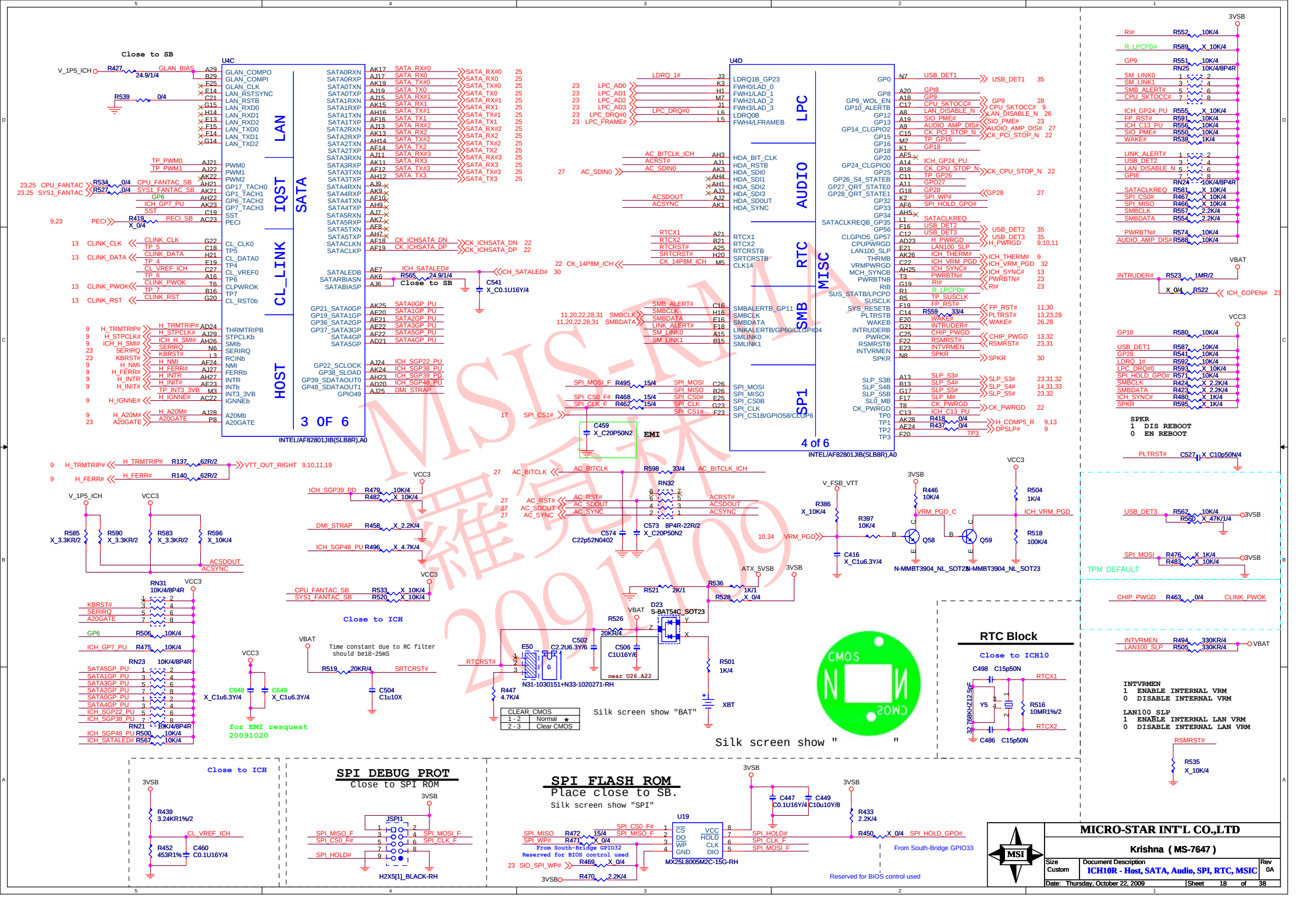
Close to SB
U4C
LAN
IQST
CL_LINK
SATA
HOST
3 OF 6
INTEL/AF82801JIB(SLB8R),A0
U4D
LPC
AUDIO
RTC
MISC
SMB
SPI
4 of 6
INTEL/AF82801JIB(SLB8R),A0
EMI
Close to ICH
for EMI resquest
20091020
Time constant due to RC filter
should be18~25mS
Silk screen show "BAT"
Silk screen show " "
RTC Block
Close to ICH10
SPI DEBUG PROT
Close to SPI ROM
SPI FLASH ROM
Place close to SB.
Silk screen show "SPI"
Reserved for BIOS control used
From South-Bridge GPIO33
MICRO-STAR INT'L CO.,LTD
Krishna (MS-7647)
ICH10R - Host, SATA, Audio, SPI, RTC, MSIC
Date: Thursday, October 22, 2009
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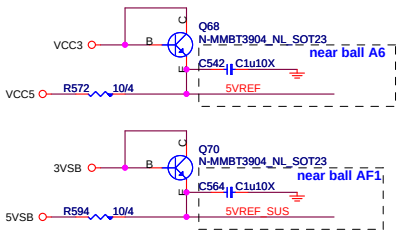
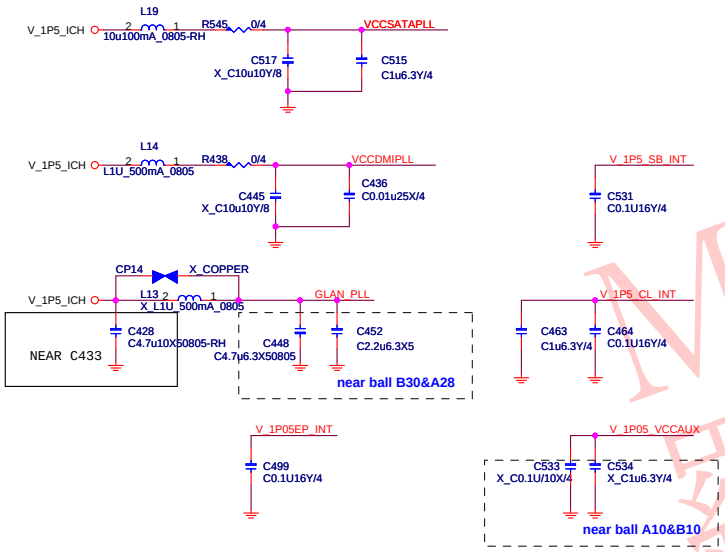
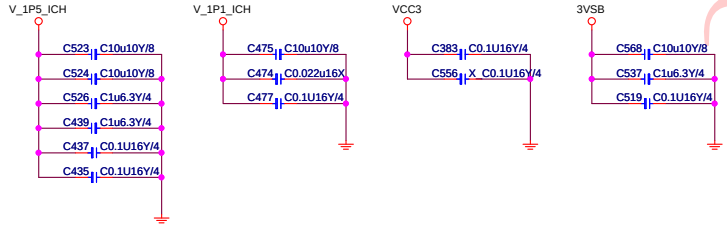
5VREF & 5VREF_SUS Sequencing Circuit

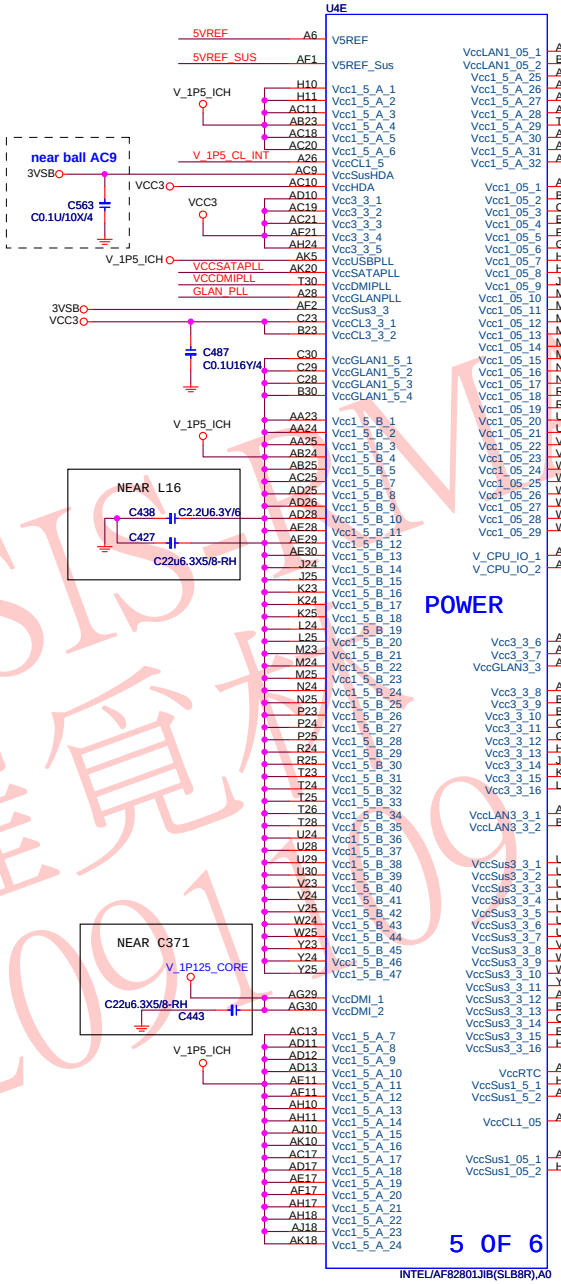
5VREF must be powered up before VCC3 or after VCC3 within 0.7V.
Also, 5VREF must power down after VCC3 or before VCC3 within 0.7V.
This rule is also applies to 5VREF_SUS and 3VSB.
However, the 3VSB is derived from the 5VSB on the power supply
thru a voltage regulator and therefore, they can satisfy the requirement.

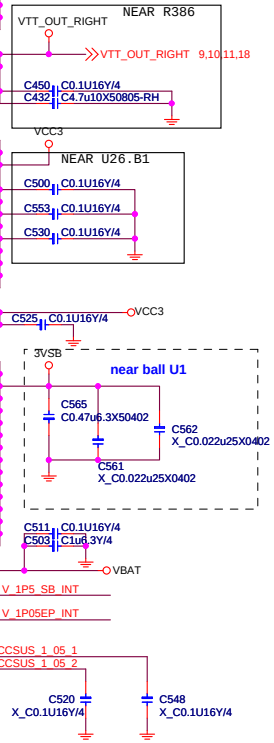


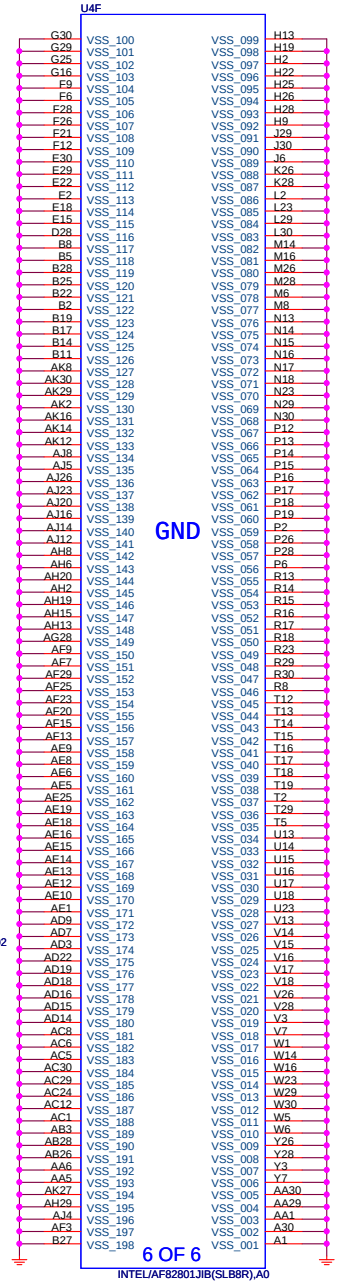
SB POWER











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Krishna (MS-7647)		
Size: Custom	Document Description: ICH10R - Power, GND	Rev: 0A
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DDRIII DIMM_A1

Silk screen show "DIMM1"

DDRIII DIMM_A2

Silk screen show "DIMM2"

DDR3

DDR3

Place close to DIMM1

Place close to DIMM1 with DIMM2

Place close to DIMM2

DDRII-240P_WHITE-RH

DDRIII-240P_BLACK-RH-2

DIMM1(CHANNEL-A)
ADDRESS = 0:0 [SA1:SA0]

DIMM2(CHANNEL-A)
ADDRESS = 0:1 [SA1:SA0]

close DIMM

close divider

MICRO-STAR INT'L CO.,LTD

Krishna (MS-7647)

Size	Document Description	Rev
C	DDR3 Chanel-A	0A

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DDRIII DIMM_B1

Silk screen show "DIMM3"

DDRIII DIMM_B2

Silk screen show "DIMM4"

DDR3

DDR3

Place close to DIMM3

Place close to DIMM3 with DIMM4

DIMM3(CHANNEL-B)
ADDRESS = 1:0 [SA1:SA0]

DIMM4(CHANNEL-B)
ADDRESS = 1:1 [SA1:SA0]

Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR_IN. When in single ended mode used for DQS0-DQS7.

Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

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Krishna (MS-7647)

Size	Document Description	Rev
C	DDR3 Chanel-B	0A

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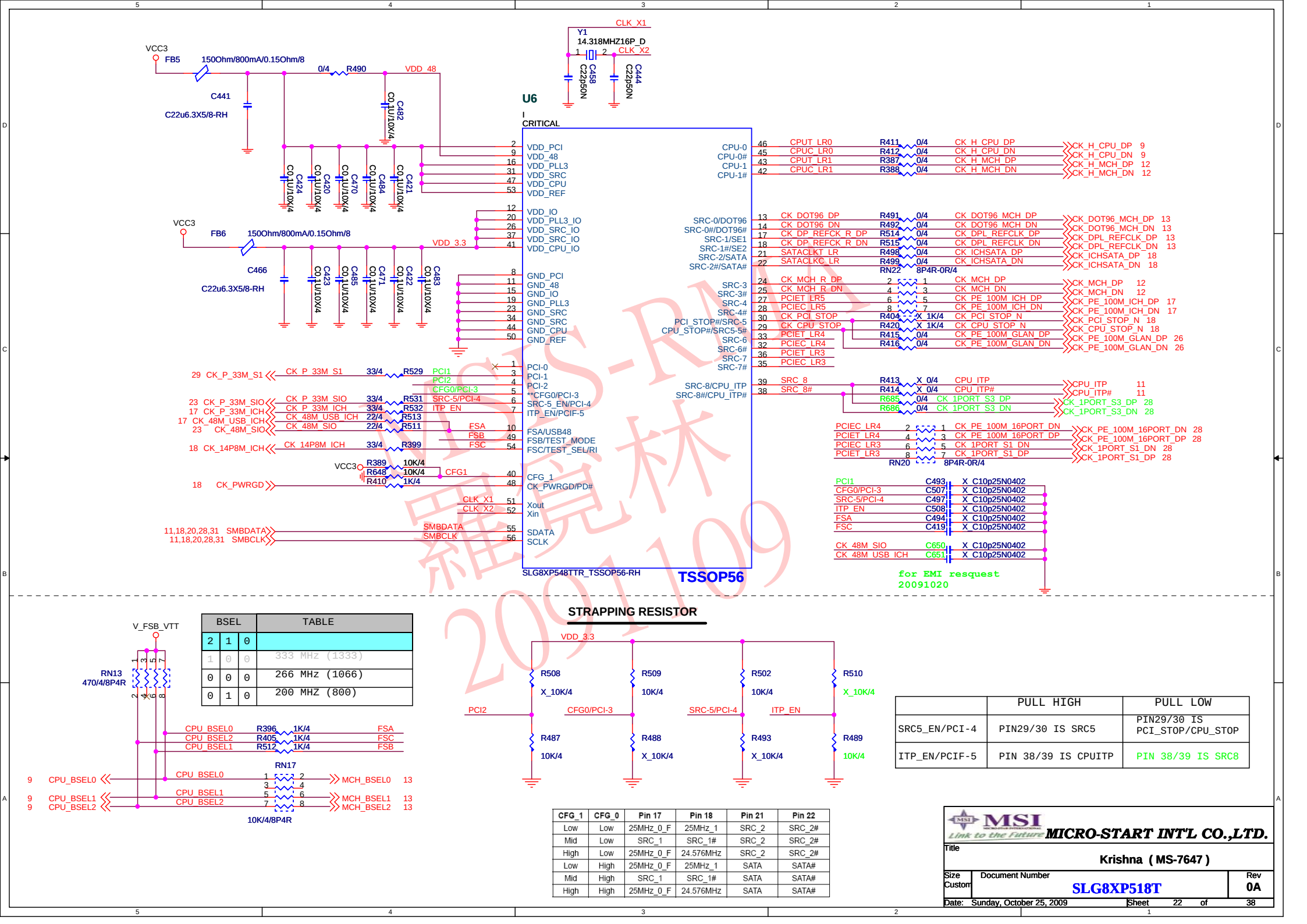
U6
SLG8XP548TTR_TSSOP56-RH
TSSOP56
Y1
14.318MHZ16P_D
STRAPPING RESISTOR
BSEL TABLE
2 1 0
1 0 0 333 MHz (1333)
0 0 0 266 MHz (1066)
0 1 0 200 MHZ (800)
PULL HIGH
PULL LOW
SRC5_EN/PCI-4
PIN29/30 IS SRC5
PIN29/30 IS PCI_STOP/CPU_STOP
ITP_EN/PCIF-5
PIN 38/39 IS CPUITP
PIN 38/39 IS SRC8
for EMI resquest 20091020
MICRO-START INT'L CO.,LTD.
Krishna (MS-7647)
SLG8XP518T
0A
Sunday, October 25, 2009
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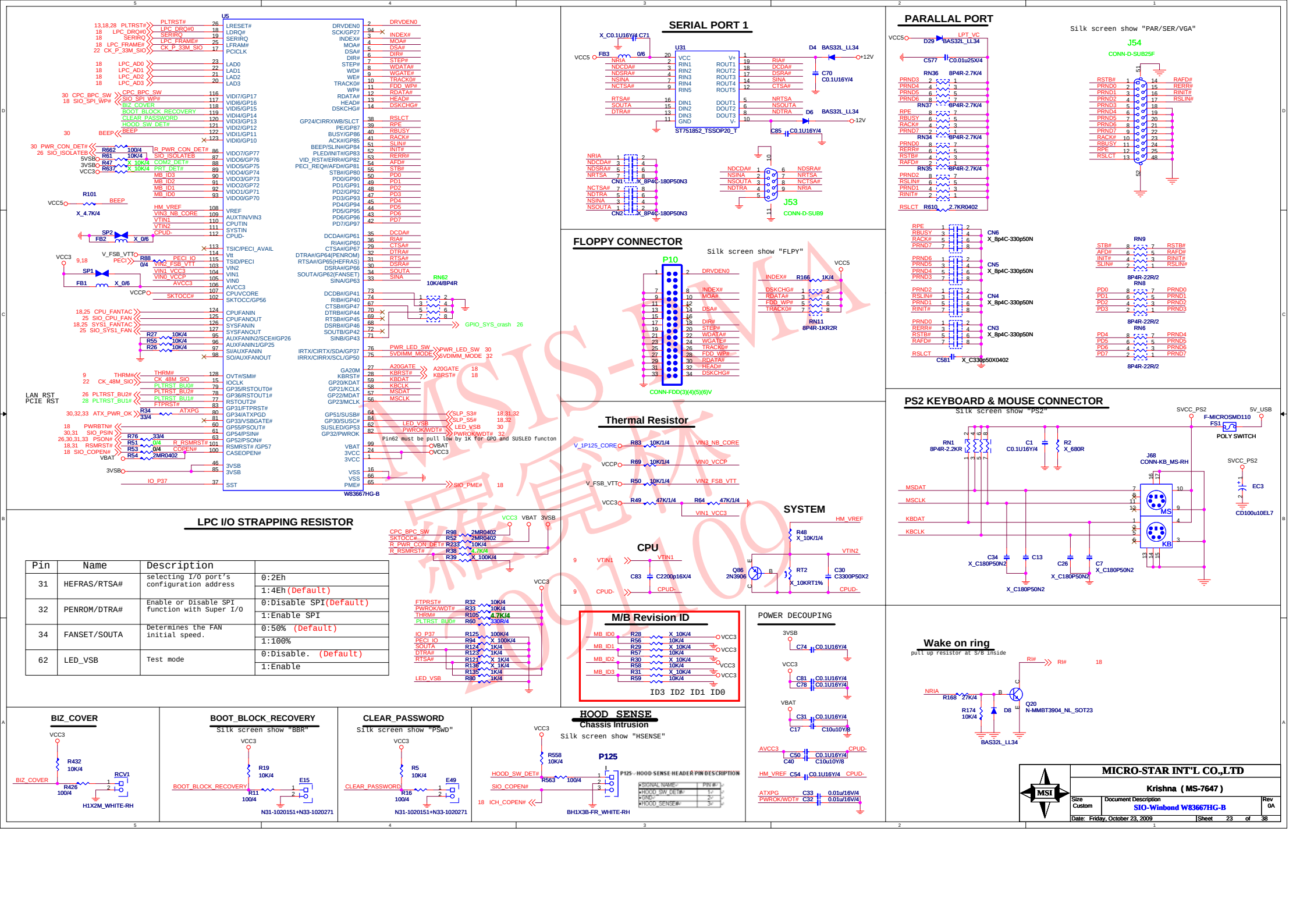
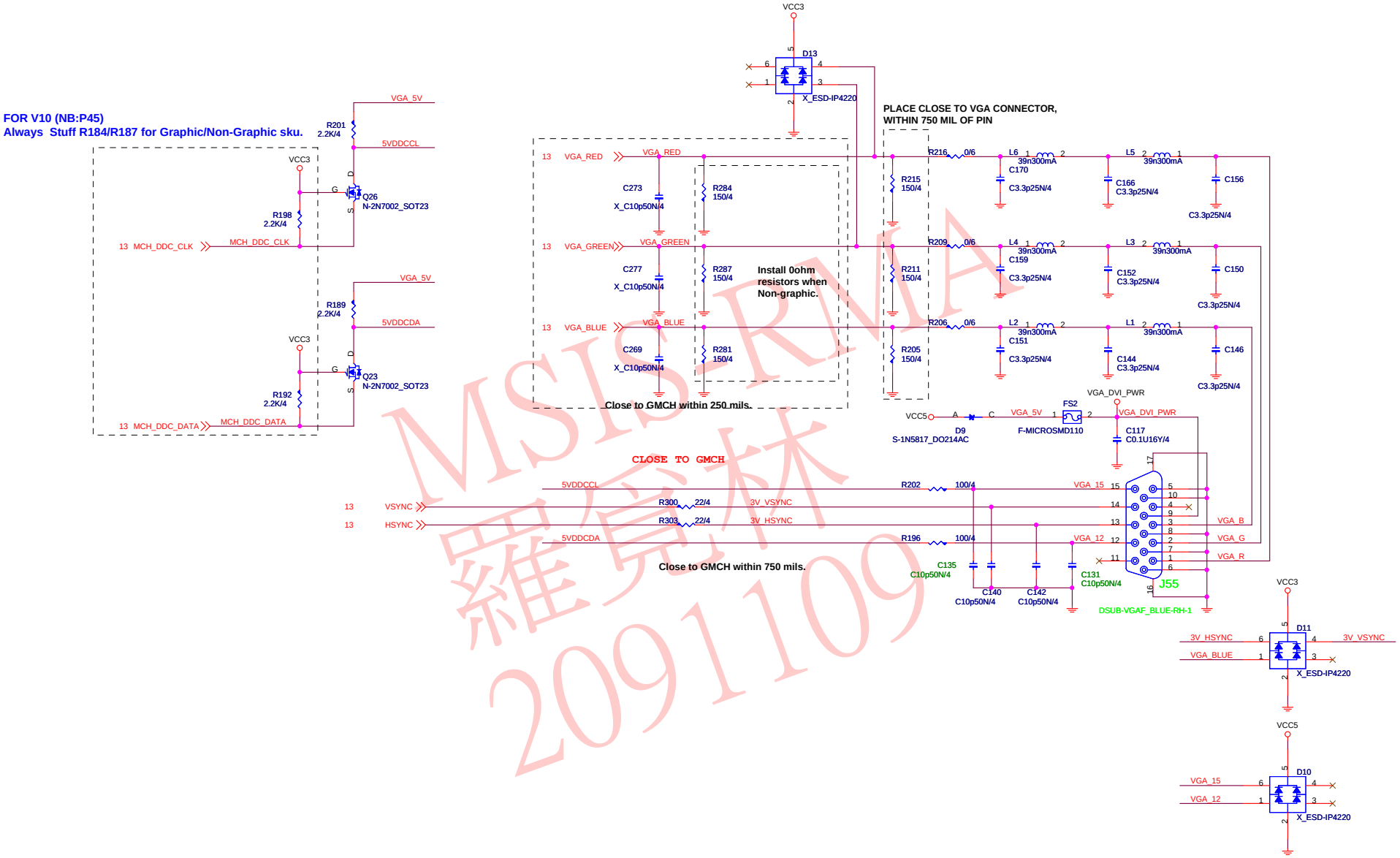


Pin	Name	Description	
31	HEFRAS/RTSA#	selecting I/O port's configuration address	0:2Eh
			1:4Eh(Default)
32	PENROM/DTRA#	Enable or Disable SPI function with Super I/O	0:Disable SPI(Default)
			1:Enable SPI
34	FANSET/SOUTA	Determines the FAN initial speed.	0:50% (Default)
			1:100%
62	LED_VSB	Test mode	0:Disable. (Default)
			1:Enable

MSI-MS
2009-10-09

Video Connector



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MSI	MICRO-STAR INT'L CO.,LTD	
	Krishna (MS-7647)	
Size: Custom	Document Description: VGA	Rev: 0A
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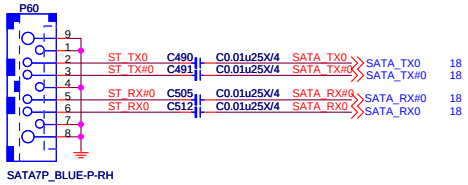
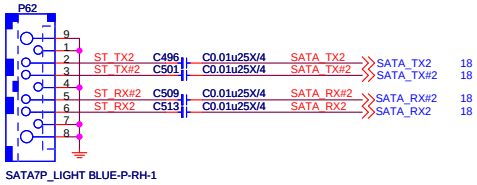
SATA 0- 3 PORT

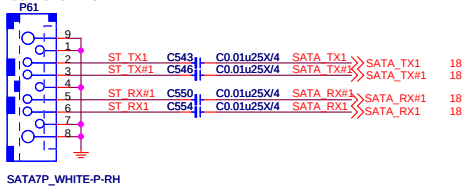
Silk screen show "SATA1"



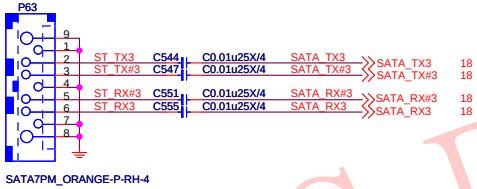
Silk screen show "SATA3"



Silk screen show "SATA2"



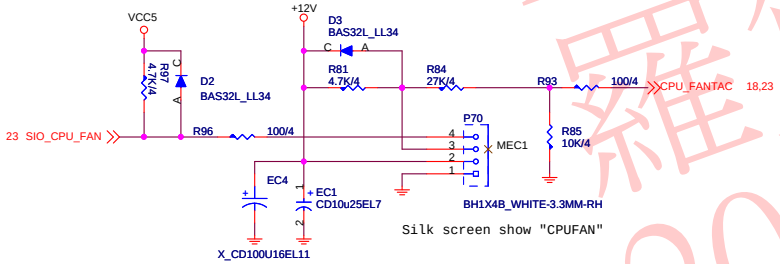
Silk screen show "SATA4"



Placement as below.

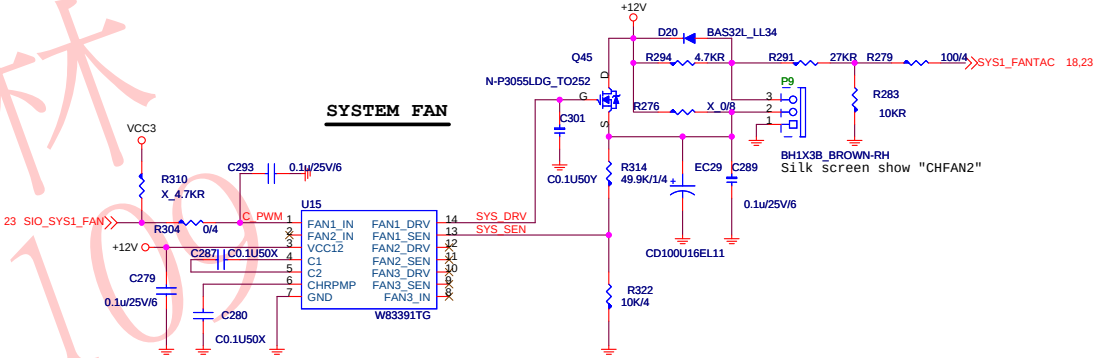
FAN-COUNTROL CIRCUIT

CPU FAN



Silk screen show "CPUFAN"

SYSTEM FAN



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MICRO-STAR INT'L CO.,LTD	
Krishna (MS-7647)	
Size: Custom	Document Description: SATA Ports and Fan Control
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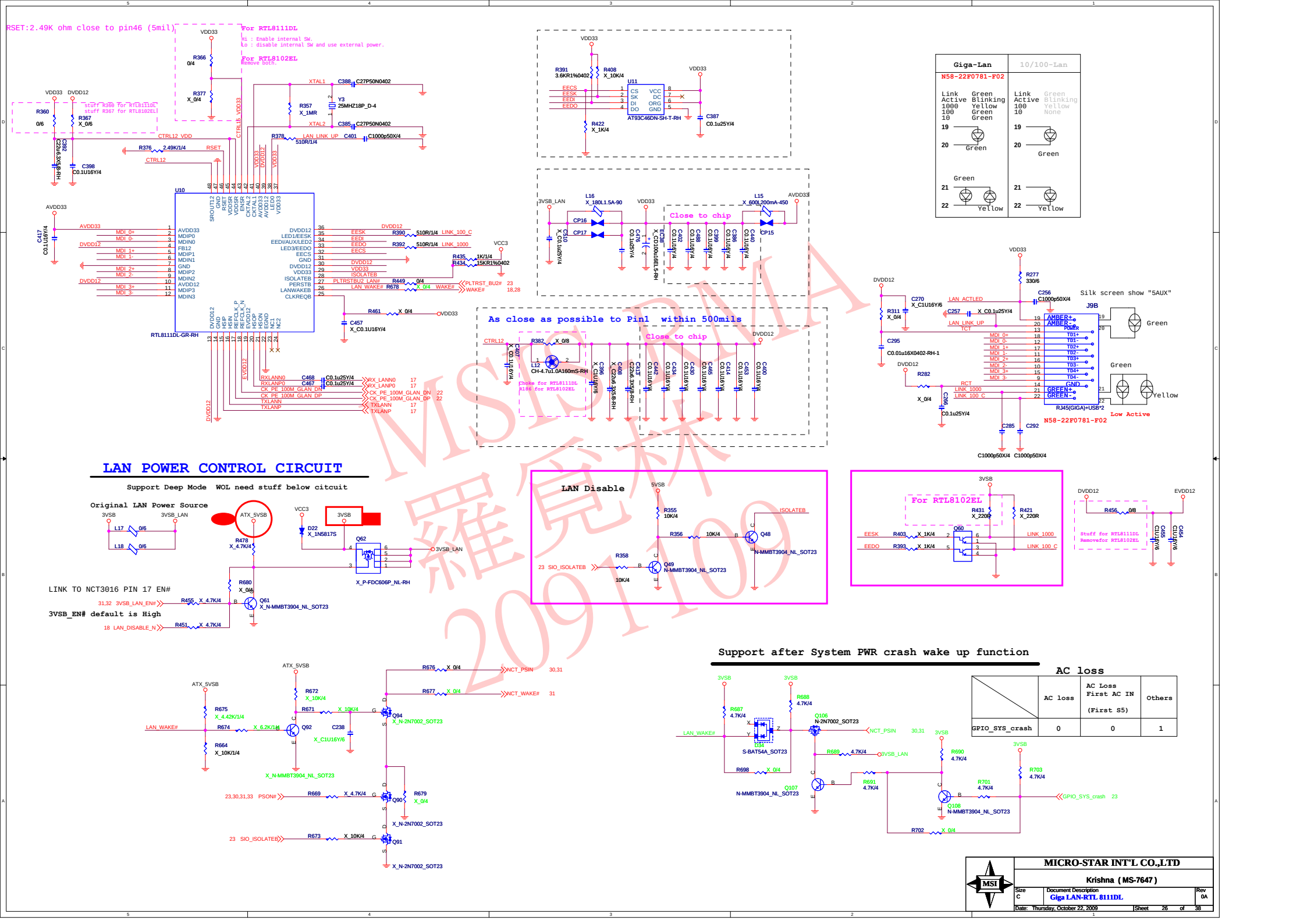
RSET:2.49K ohm close to pin46 (5mil)
For RTL8111DL
Hi : Enable internal SW.
Lo : disable internal SW and use external power.
For RTL8102EL
Remove both.
stuff R360 for RTL8111DL
stuff R367 for RTL8102EL
RTL8111DL-GR-RH
As close as possible to Pin1 within 500mils
Close to chip
Choke for RTL8111DL
R166 for RTL8102EL
Giga-Lan
N58-22F0781-F02
10/100-Lan
Silk screen show "5AUX"
Low Active
LAN POWER CONTROL CIRCUIT
Support Deep Mode WOL need stuff below citcuit
Original LAN Power Source
LINK TO NCT3016 PIN 17 EN#
3VSB_EN# default is High
LAN Disable
For RTL8102EL
Support after System PWR crash wake up function
AC loss
AC loss
AC Loss First AC IN (First S5)
Others
GPIO_SYS_crash
MICRO-STAR INT'L CO.,LTD
Krishna (MS-7647)
Giga LAN-RTL 8111DL
Thursday, October 22, 2009
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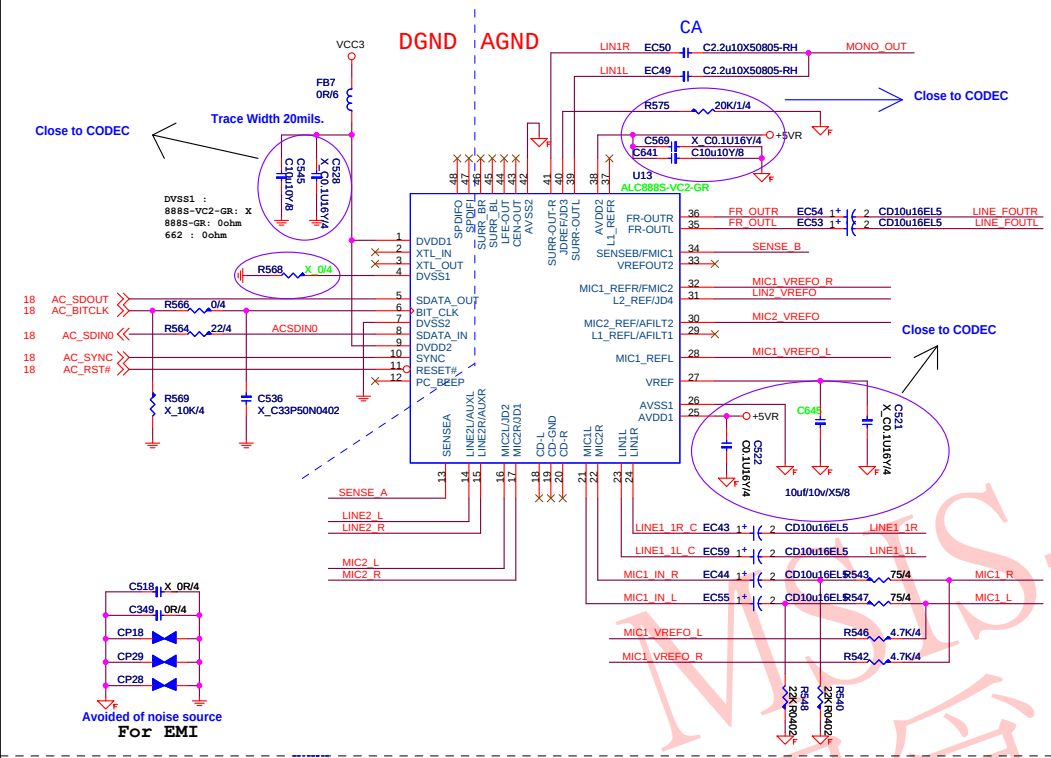
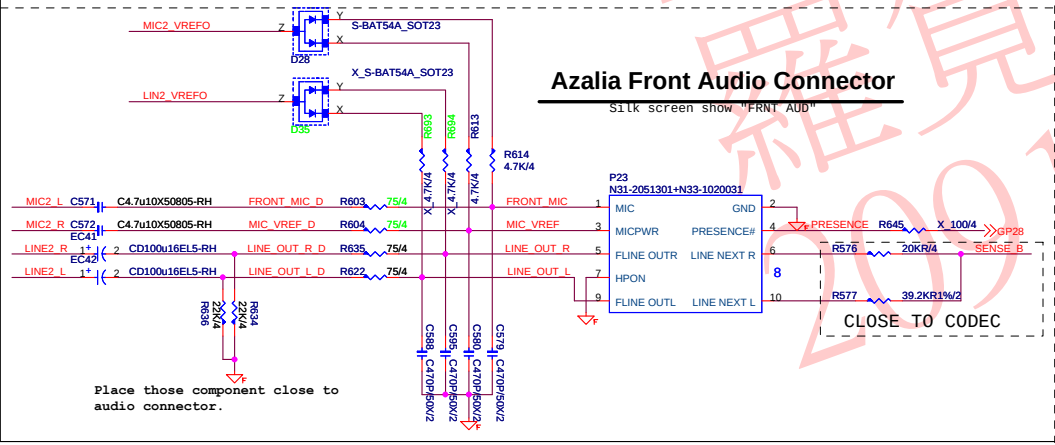
ALC888S-VC2-GR CODEC

Support 8.1 channel





Azalia Front Audio Connector

Silk screen show "FRNT AUD"

ALC888S_VC2 JACK

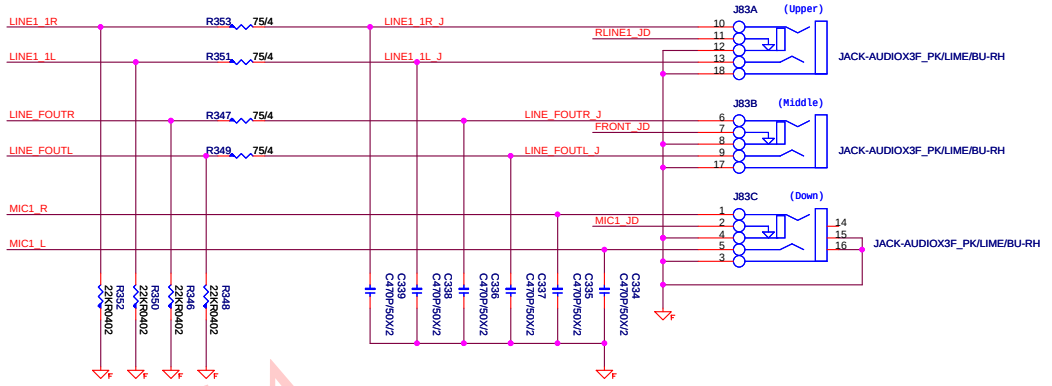
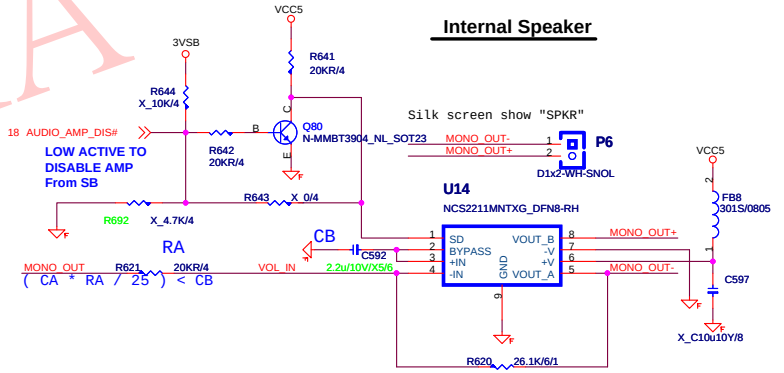


TABLE 14
SPEAKER HEADER DEFINITION

P6

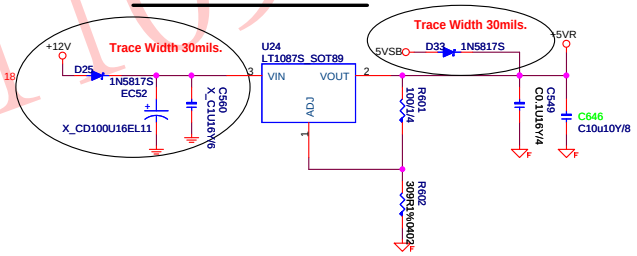
SPEAKER-	1
SPEAKER+	2

Internal Speaker



U14 at Layer1 & 4 need increase copper for thermal

AUDIO CODE REGULATORS



ALC888S_VC2 JACK DETECT

MICRO-STAR INT'L CO.,LTD		
Krishna (MS-7647)		
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MSI-RMA 羅覺林 20091109

PCI Express X16 Slot

Silk screen show "X16PCIEXP"

Trace width > 200 mils

13,18,23 PLTRST# — R695 X_0/4 — R696 0/4 — PLTRST_BU1# 23

PLTRST_BU1R#

+12V, VCC3, +3.3V_SLOT

SMBCLK, SMBDATA, WAKE#, SDVO_CTRL_CLK, SDVO_CTRL_DATA, EXP16_PRSNT#, DDCP_CTRLDATA, DDCP_CTRLCLK 13

PRSNT1#, PRSNT2#1, PRSNT2#2, PRSNT2#3, PRSNT2#4

JTAG1, JTAG2, JTAG3, JTAG4, JTAG5, PWRGD, 3.3VAUX, 3.3V

CK_PE_100M_16PORT_DP, CK_PE_100M_16PORT_DN

EXP_A_TXP_0 C381 C0.1U16X0402 EXP_A_TXP_0_C

EXP_A_TXN_0 C380 C0.1U16X0402 EXP_A_TXN_0_C

EXP_A_TXP_1 C351 C0.1U16X0402 EXP_A_TXP_1_C

EXP_A_TXN_1 C350 C0.1U16X0402 EXP_A_TXN_1_C

EXP_A_TXP_2 C372 C0.1U16X0402 EXP_A_TXP_2_C

EXP_A_TXN_2 C371 C0.1U16X0402 EXP_A_TXN_2_C

EXP_A_TXP_3 C375 C0.1U16X0402 EXP_A_TXP_3_C

EXP_A_TXN_3 C374 C0.1U16X0402 EXP_A_TXN_3_C

EXP_A_TXP_4 C373 C0.1U16X0402 EXP_A_TXP_4_C

EXP_A_TXN_4 C352 C0.1U16X0402 EXP_A_TXN_4_C

EXP_A_TXP_5 C354 C0.1U16X0402 EXP_A_TXP_5_C

EXP_A_TXN_5 C353 C0.1U16X0402 EXP_A_TXN_5_C

EXP_A_TXP_6 C377 C0.1U16X0402 EXP_A_TXP_6_C

EXP_A_TXN_6 C376 C0.1U16X0402 EXP_A_TXN_6_C

EXP_A_TXP_7 C379 C0.1U16X0402 EXP_A_TXP_7_C

EXP_A_TXN_7 C378 C0.1U16X0402 EXP_A_TXN_7_C

EXP_A_TXP_8 C355 C0.1U16X0402 EXP_A_TXP_8_C

EXP_A_TXN_8 C356 C0.1U16X0402 EXP_A_TXN_8_C

EXP_A_TXP_9 C357 C0.1U16X0402 EXP_A_TXP_9_C

EXP_A_TXN_9 C358 C0.1U16X0402 EXP_A_TXN_9_C

EXP_A_TXP_10 C360 C0.1U16X0402 EXP_A_TXP_10_C

EXP_A_TXN_10 C359 C0.1U16X0402 EXP_A_TXN_10_C

EXP_A_TXP_11 C362 C0.1U16X0402 EXP_A_TXP_11_C

EXP_A_TXN_11 C361 C0.1U16X0402 EXP_A_TXN_11_C

EXP_A_TXP_12 C363 C0.1U16X0402 EXP_A_TXP_12_C

EXP_A_TXN_12 C364 C0.1U16X0402 EXP_A_TXN_12_C

EXP_A_TXP_13 C366 C0.1U16X0402 EXP_A_TXP_13_C

EXP_A_TXN_13 C365 C0.1U16X0402 EXP_A_TXN_13_C

EXP_A_TXP_14 C368 C0.1U16X0402 EXP_A_TXP_14_C

EXP_A_TXN_14 C367 C0.1U16X0402 EXP_A_TXN_14_C

EXP_A_TXP_15 C370 C0.1U16X0402 EXP_A_TXP_15_C

EXP_A_TXN_15 C369 C0.1U16X0402 EXP_A_TXN_15_C

EXP_A_RXP_0 … EXP_A_RXP_15, EXP_A_RXN_0 … EXP_A_RXN_15

SLOT-PCI164P_BLACK-2PITCH-RH-21

PCI Express X1 Slot

Silk screen show "X1PCEXP1"

J31

+12V, VCC3, +3.3V_SLOT, SMBCLK, SMBDATA, WAKE#, PLTRST_BU1R#

PE_TXP 17, PE_TXN 17

CK_1PORT_S1_DP, CK_1PORT_S1_DN

PE_RXP1 17, PE_RXN1 17

SLOT-PCI36P_BLACK-2PITCH-RH-10

EC35 CD470u16EL11.5-RH

PCI Express X1 Slot

Silk screen show "X1PCEXP2"

J32

+12V, VCC3, +3.3V_SLOT, SMBCLK, SMBDATA, WAKE#, PLTRST_BU1R#

PE_TXP3 17, PE_TXN3 17

CK_1PORT_S3_DP, CK_1PORT_S3_DN

PE_RXP3 17, PE_RXN3 17

SLOT-PCI36P_BLACK-2PITCH-RH-10

+3.3V_SLOT

3VSB, +3.3V_SLOT

RN61 8P4R-0R/6

R524 X_4.7K/4

U25 X_APL3511BBI-TRG_SOT23-5-HF

SLOT_EN#

18 GP9 — R663 X_10K/4 — Q105 X_N-MMBT3904_NL_SOT23

EC70 X_CD100u16EL5-RH, C642 X_0.1uF/16V/X7R/6

MSI-RMA 客戶編號 091109

MICRO-STAR INT'L CO.,LTD

Krishna (MS-7647)

Size	Document Description	Rev
Custom	PCIE x16 & x1 Slots 1 & 2	0A

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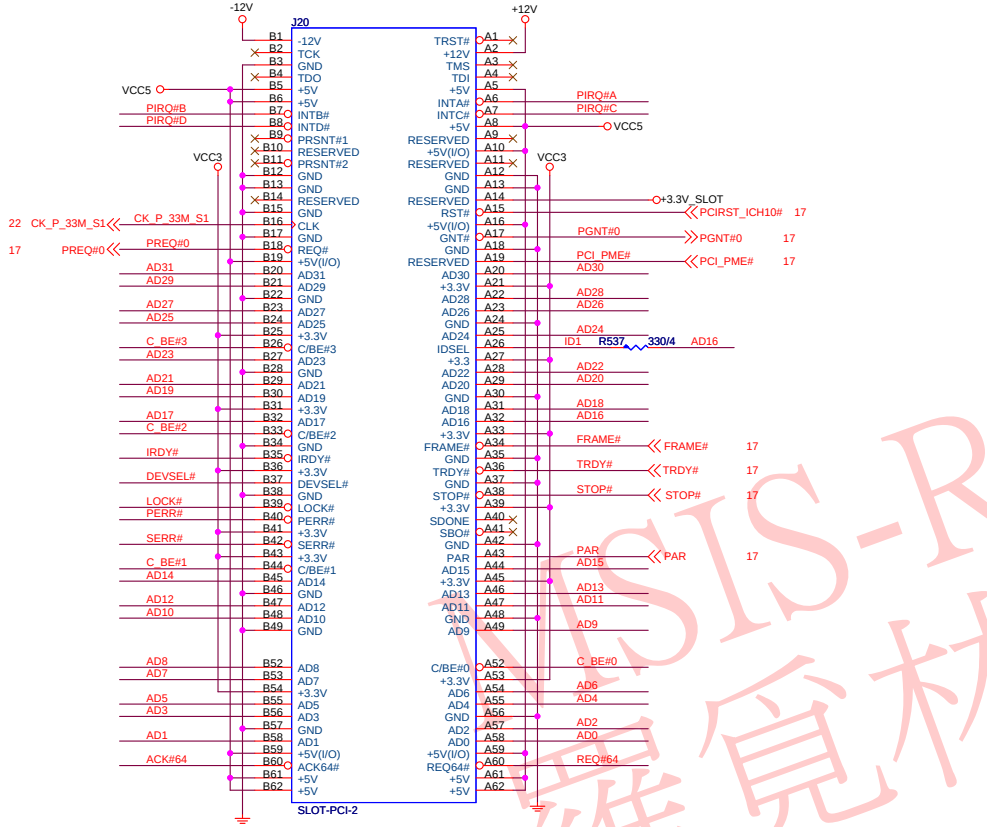
PCI SLOT 1 (PCI VER: 2.2 COMPLY)

Silk screen show "PCI1"

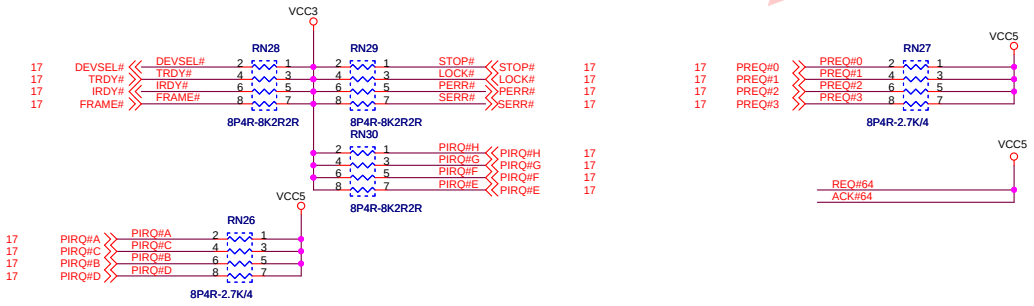


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

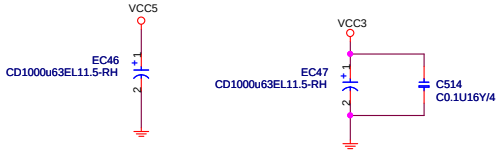
17 AD[31..0] AD[31..0]

17 C_BE#[3..0] C_BE#[3..0]

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS



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Krishna (MS-7647)		
Size: Custom	Document Description: PCI Slot 1	Rev: 0A
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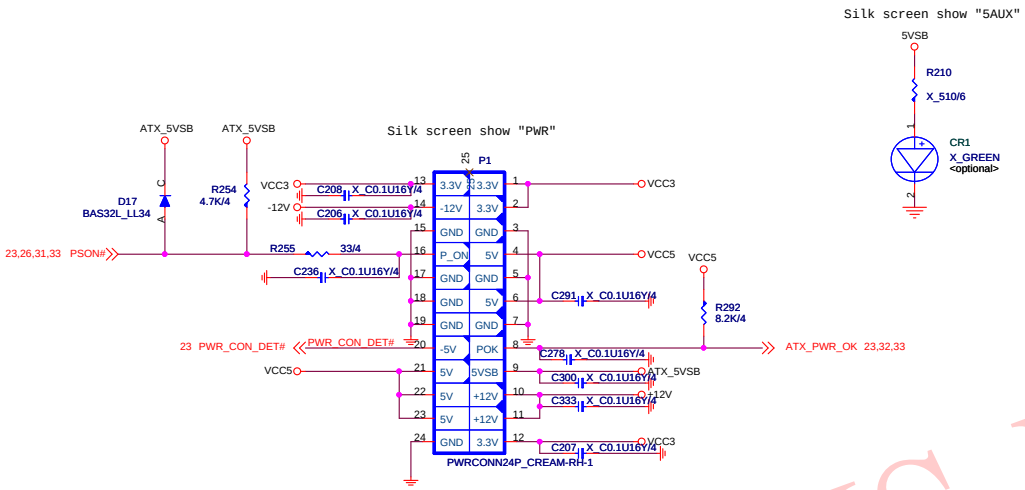
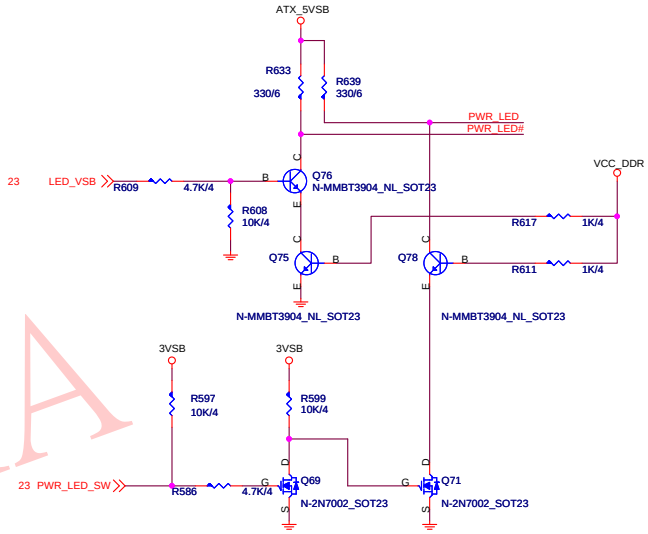
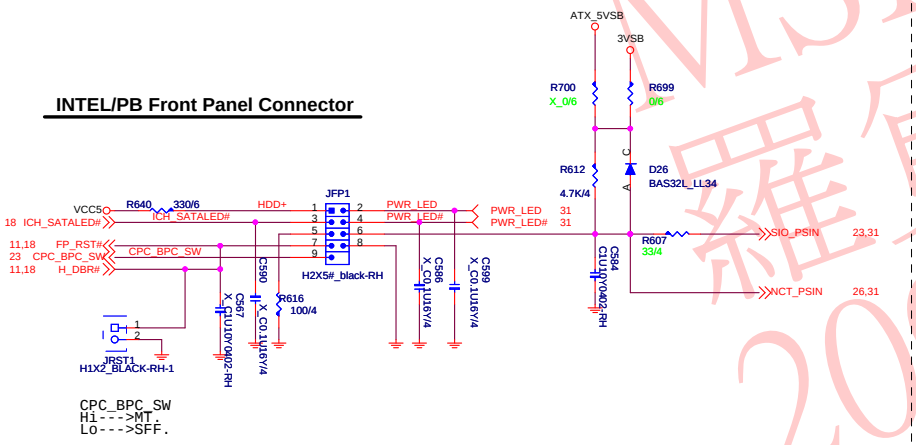
ATX POWER CONNECTOR



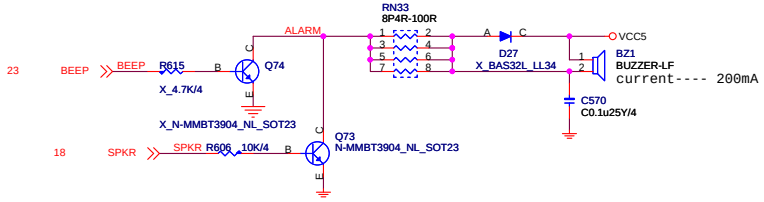
LED (for W83667)



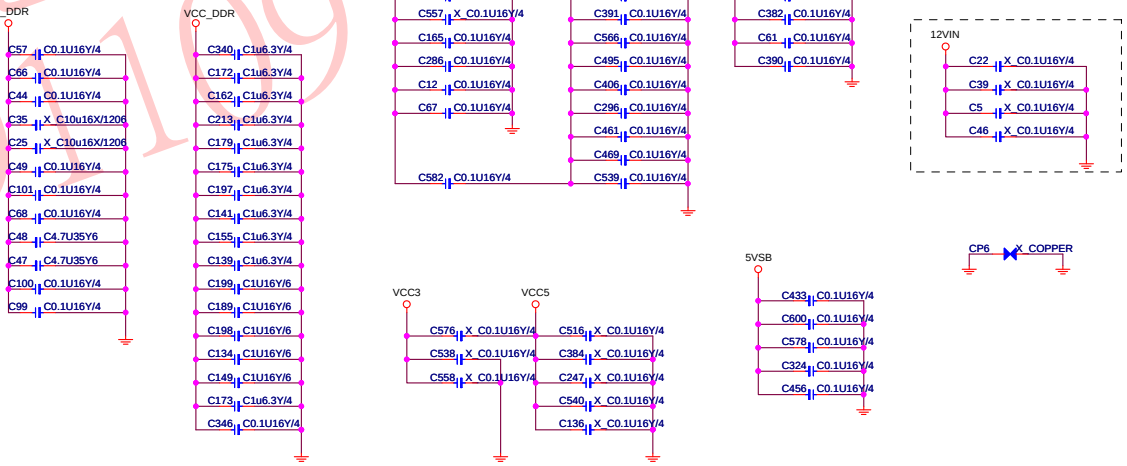
INTEL/PB Front Panel Connector



Buzzer

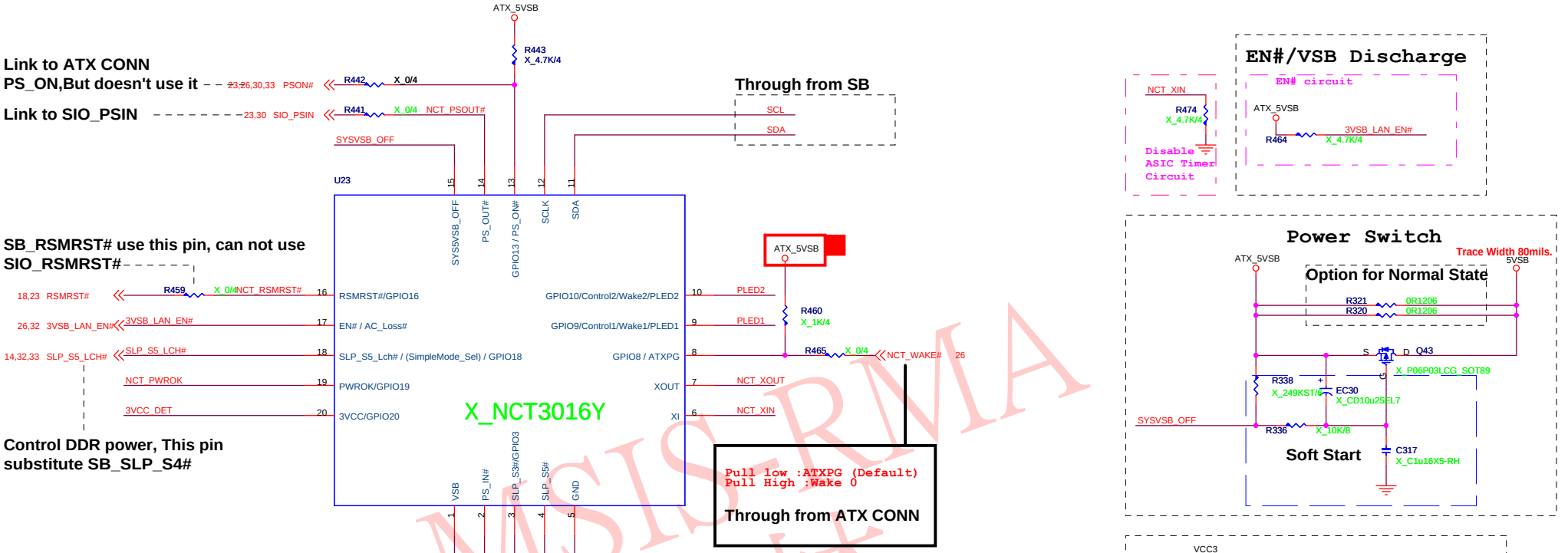


Cap. for EMI & Power



MSIS-RMA 羅宣林 2009199

MICRO-STAR INT'L CO.,LTD	
Krishna (MS-7647)	
Size: Custom	Document Description: ATX PWR-Connector & Front Panel
Rev: 0A	
Date: Thursday, October 22, 2009	Sheet 30 of 38



POWER ON STRAPPING PIN

PIN	Name	0	1
18	SimpleMode_Sel	Full function	Simple Mode

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MICRO-STAR INT'L CO.,LTD

Krishna (MS-7647)

Size: Custom | Document Description: Advance power NCT3016Y | Rev: 0A

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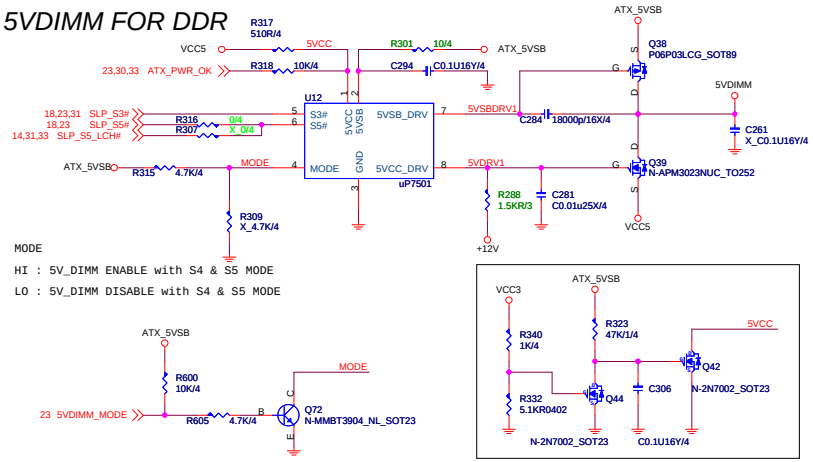
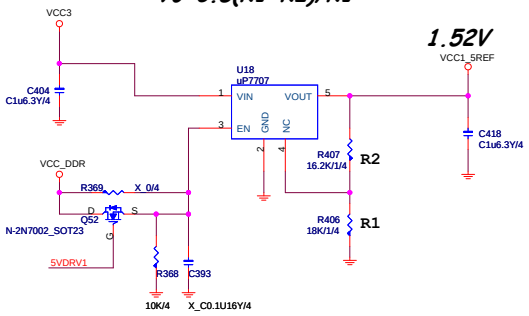
5VDIMM FOR DDR

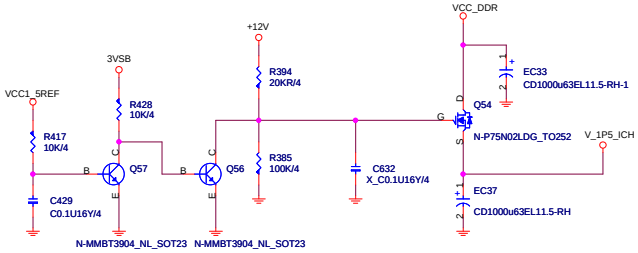


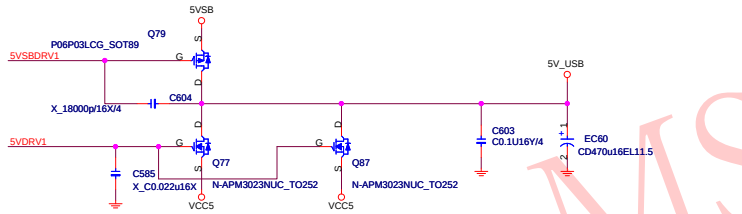
VCC1.5REF

Vo=0.8(R1+R2)/R1

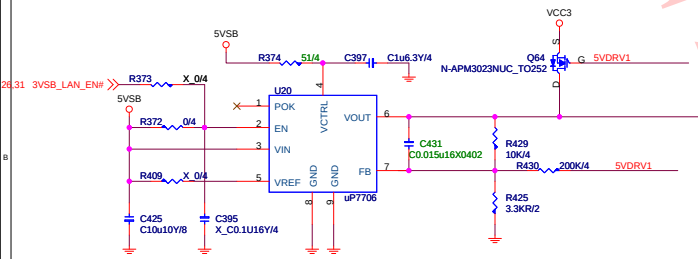


SB 1.5V 2.4A

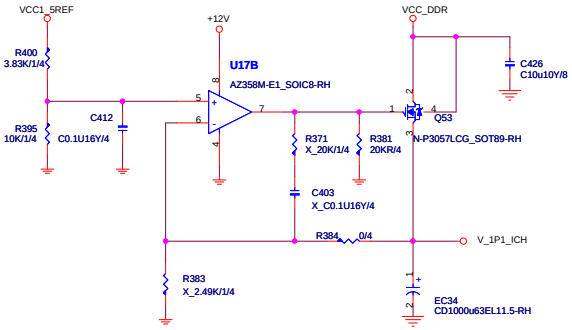




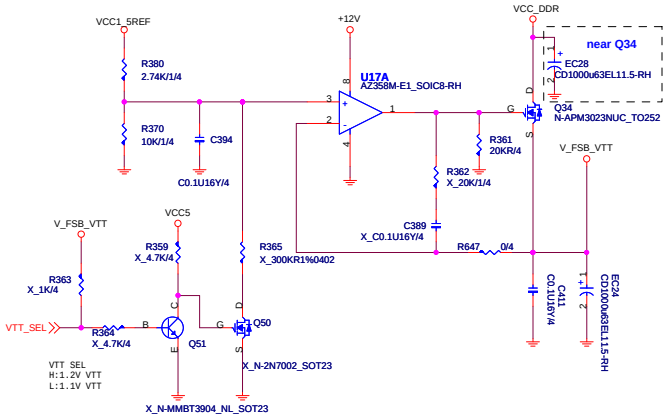
3VSB

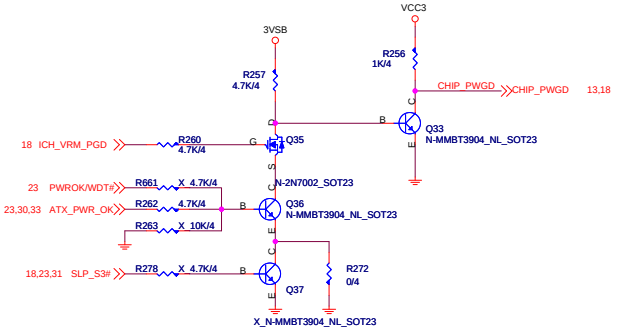


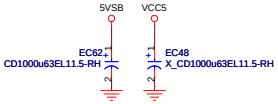
SB 1.1V 1.16A



1.2V 5.8A







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209109

MICRO-STAR INT'L CO.,LTD

Krishna (MS-7647)

Size	Document Description	Rev
Custom	ACPI controller UPI	0A

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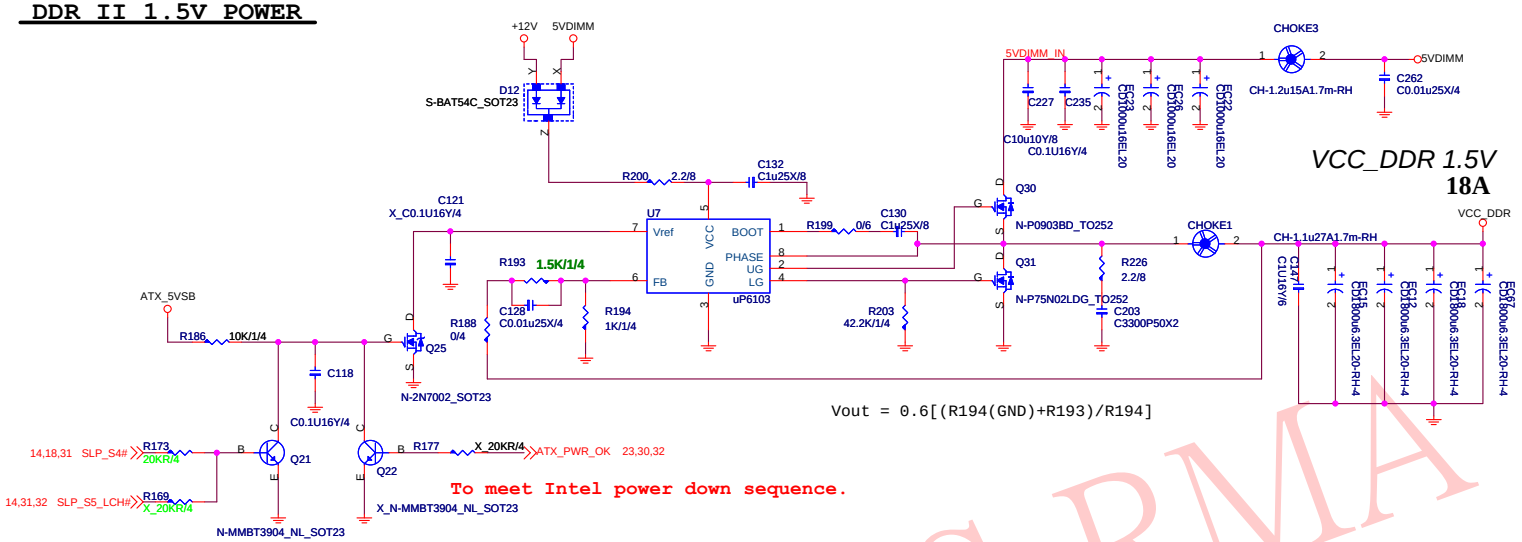
DDR II 1.5V POWER



Vout = 0.6[(R194(GND)+R193)/R194]

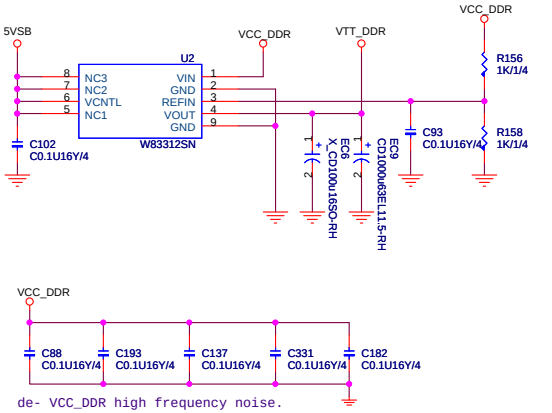
To meet Intel power down sequence.

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

DDR VTT Power

VTT_DDR 0.75V

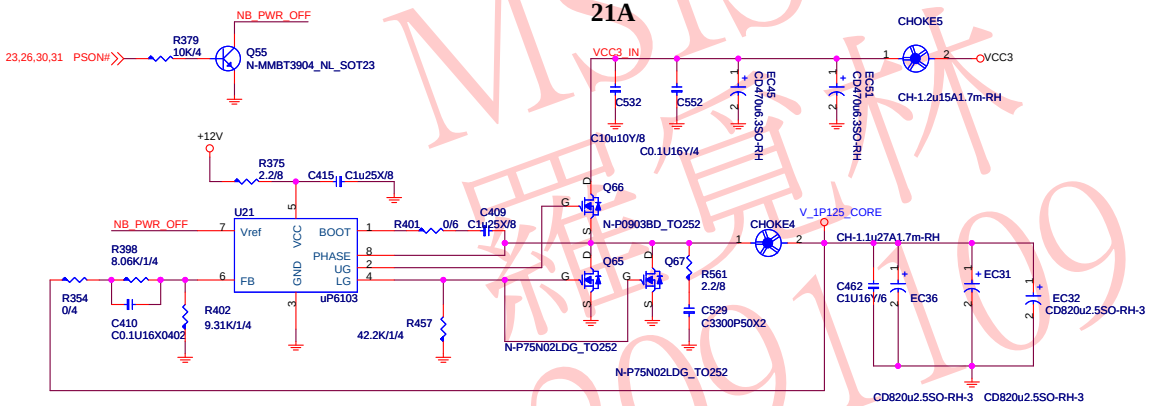
0.83A



de- VCC_DDR high frequency noise.

NB 1.125V POWER

21A



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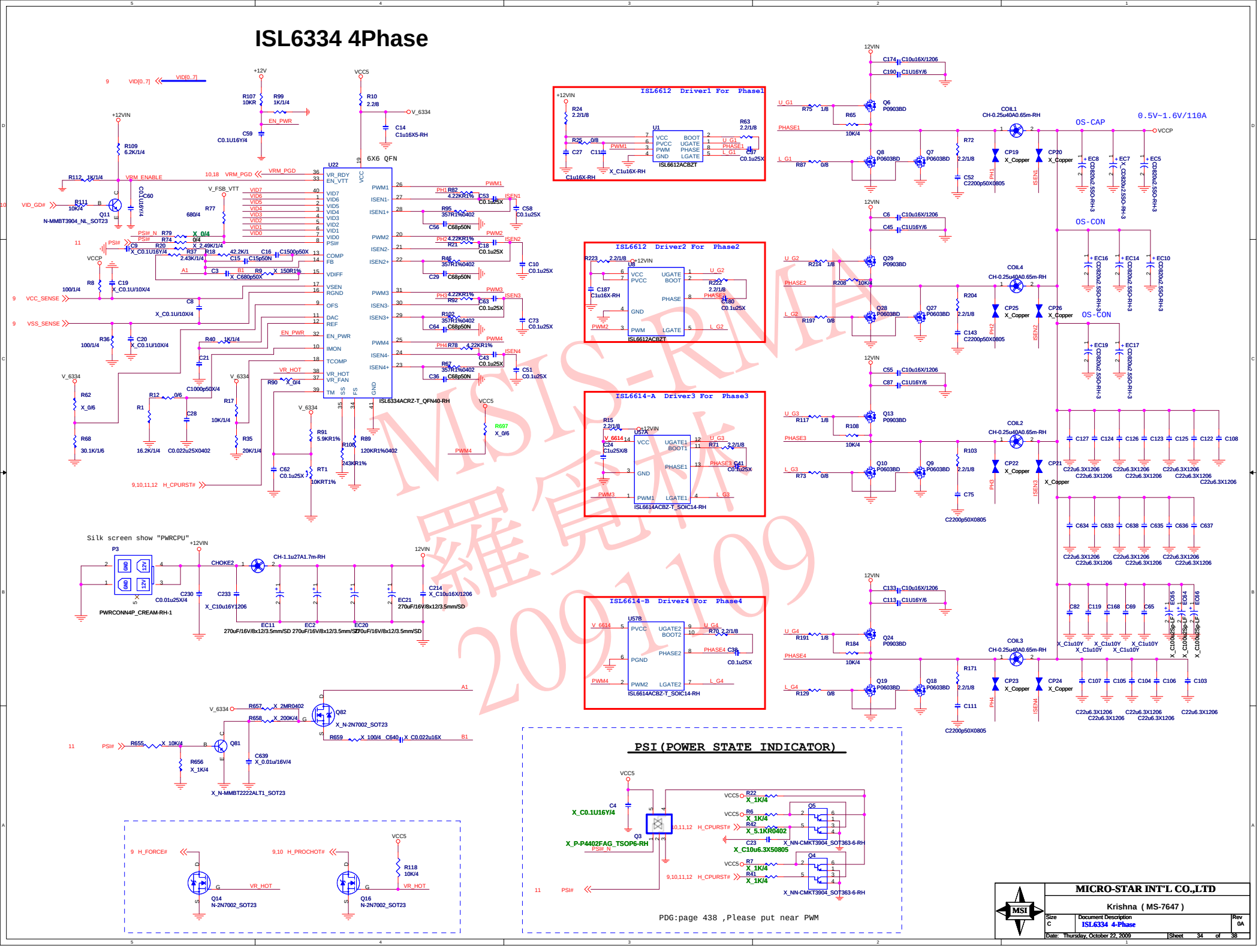
ISL6334 4Phase



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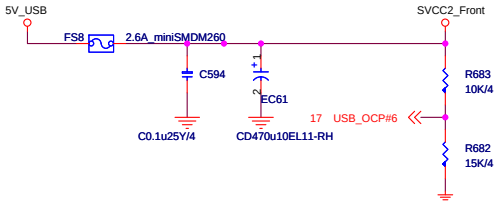
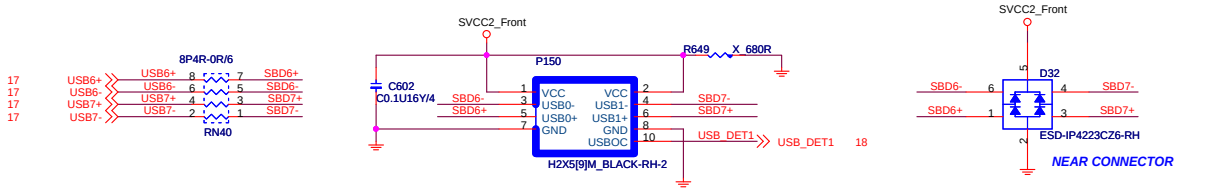
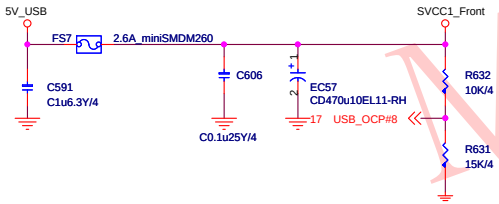
Front USB Connector



FRONT USB PORT6,7

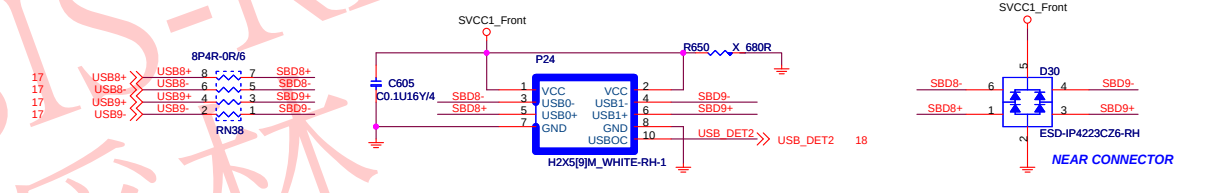
Silk screen show "MEDIA"

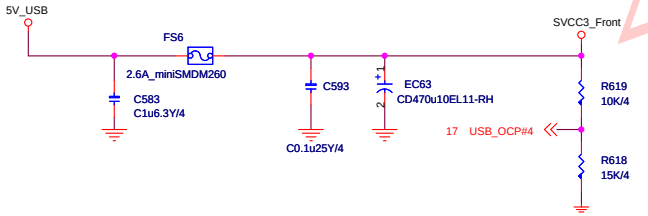




FRONT USB PORT 8,9

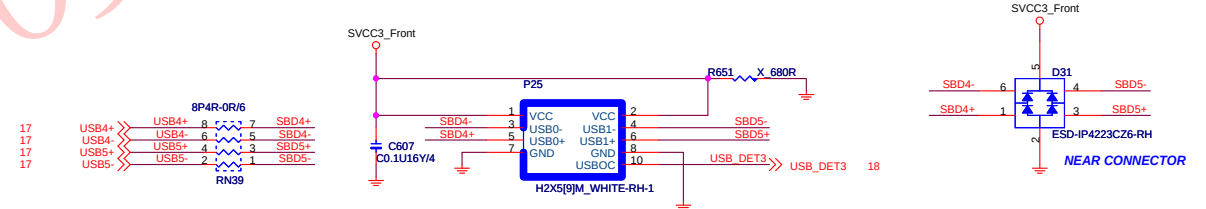
Silk screen show "FRNT USB"





FRONT USB PORT 4,5

Silk screen show "IUSB1"



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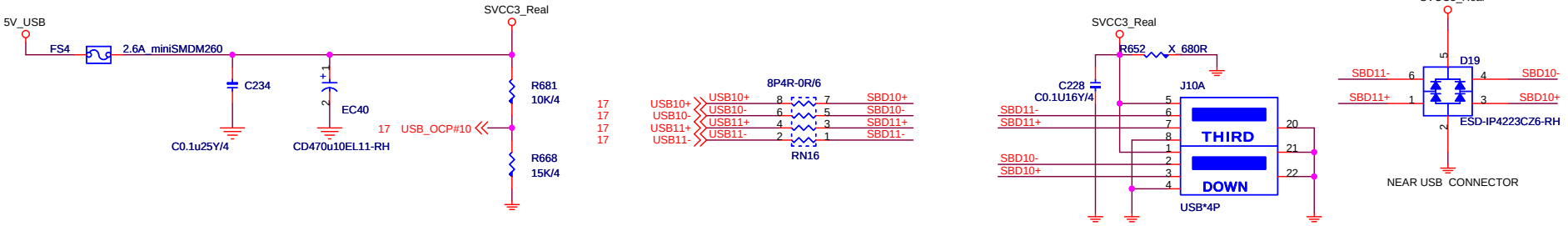
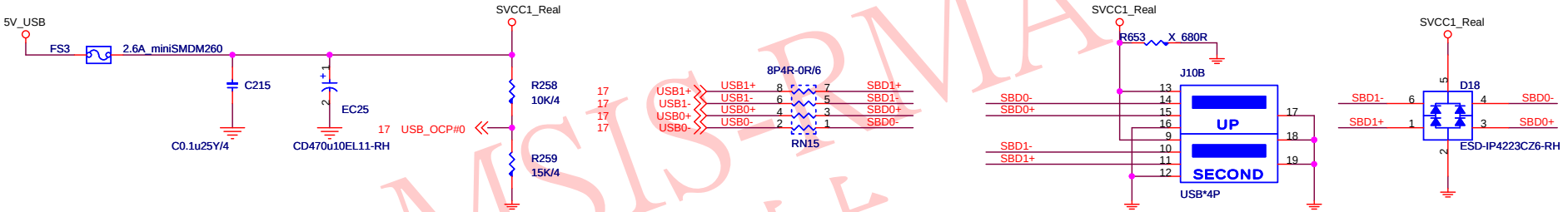
Rear USB Connector

REAR USB PORT 0,1,10,11

Silk screen show "USB"

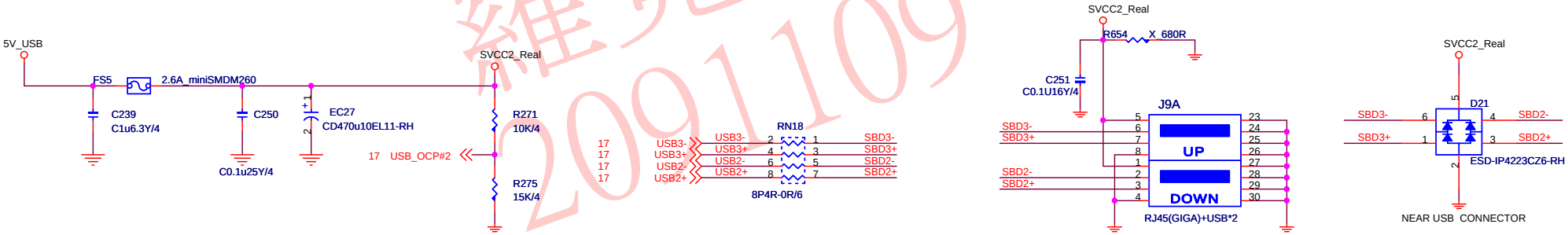


Silk screen show "USB"



REAR USB PORT 2,3 (With LAN)

Silk screen show "RJ45/USB"



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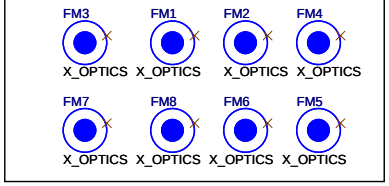
crisscross Optical Marks



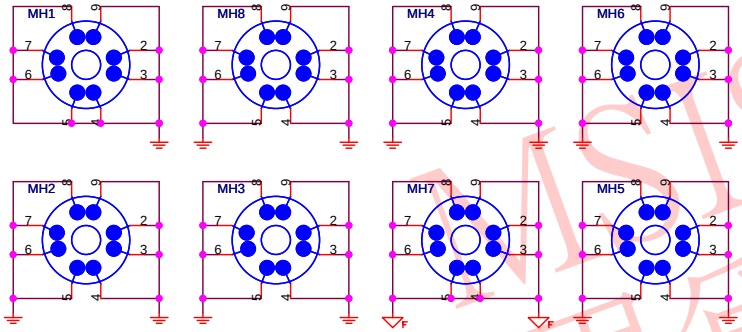
PCB1

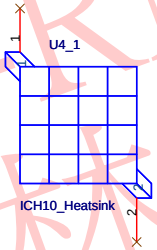
7647-0A

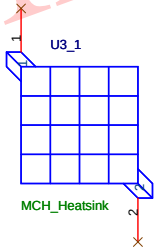
BAT

BATTERY-CR2032

Mounting Holes



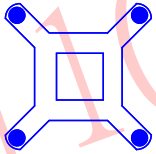




E31-0401630-E25,PUSH PIN

E31-0401900-K08,NON PUSH PIN

XU1_1

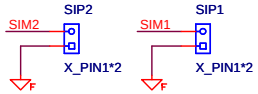


BACK-PLATE

LAB1

AMI BIOS Label

Simulation



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ICH10R

GPIO	Alt Func	I/O/NC	Power	Tol	Default	Signal Name
GPIO[0]	BM_BUSY#	I/O	Core	3.3V	GPI	USB_DET1
GPIO[1]	TACH1	I/O	Core	3.3V	GPI	SYS1_FANTAC
GPIO[5:2]	PIRQ[H:E]#	I/OD	Core	5V	GPI	PIRQ#[H:E]
GPIO[7:6]	TACH[3:2]	I/O	Core	3.3V	GPI	
GPIO[8]	unmuxed	I/O	Resume	3.3V	GPI	
GPIO[9]	WOL_EN	I/O	Resume	3.3V	Native	GP9(SLOT power)
GPIO[10]	CLGPIO1	I/O	Resume	3.3V	GPI	CPU_SKTOCC#
GPIO[11]	SMBALERT#	I/O	Resume	3.3V	Native	
GPIO[12]	unmuxed	I/O	Resume	3.3V	GPO	LAN_DISABLE
GPIO[13]	unmuxed	I/O	Resume	3.3V	GPI	SIO_PME#
GPIO[14]	CLGPIO2	I/O	Resume	3.3V	GPI	AUDIO_AMP_DIS#
GPIO[15]	unmuxed	I/O	Resume	3.3V	Native	CK_PCI_STOP_N
GPIO[16]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[17]	TACH0	I/O	Core	3.3V	GPI	CPU_FANTAC
GPIO[18]	unmuxed	I/O	Core	3.3V	GPO	
GPIO[19]	SATA1GP	I/O	Core	3.3V	GPI	SATA1GP_PU
GPIO[20]	unmuxed	I/O	Core	3.3V	GPO	R_DIS_TCM#
GPIO[21]	SATA0GP	I/O	Core	3.3V	GPI	SATA0GP_PU
GPIO[22]	SCLOCK	I/O	Core	3.3V	GPI	ICH_SGP22_PU
GPIO[23]	LDRQ1#	I/O	Core	3.3V	Native	LDRQ_1#
GPIO[24]	CLGPIO0	I/O	Resume	3.3V	GPO	ICH_GP24_PU
GPIO[25]	STP_CPU#	I/O	Resume	3.3V	Native	CK_CPU_STOP_N
GPIO[26]	S4_STATE#	I/O	Resume	3.3V	Native	TP_GP26
GPIO[27]	QRT_STATE0	I/O	Resume	3.3V	GPO	GPO27
GPIO[28]	QRT_STATE1	I/O	Resume	3.3V	GPO	GP28(AUDIO_PRESENCE)
GPIO[29]	OC5#	I/O	Resume	3.3V	Native	OC#4
GPIO[30]	OC6#	I/O	Resume	3.3V	Native	OC#6
GPIO[31]	OC7#	I/O	Resume	3.3V	Native	OC#6
GPIO[32]	unmuxed	I/O	Core	3.3V	GPO	SPI_WP#
GPIO[33]	unmuxed	I/O	Core	3.3V	GPO	SPI_HOLD_GPO#
GPIO[34]	unmuxed	I/O	Core	3.3V	GPO	R_DIS_TPM#
GPIO[35]	SATACLKREQ#	I/O	Core	3.3V	GPO	
GPIO[36]	SATA2GP	I/O	Core	3.3V	GPI	SATA2GP_PU
GPIO[37]	SATA3GP	I/O	Core	3.3V	GPI	SATA3GP_PU
GPIO[38]	SLOAD	I/O	Core	3.3V	GPI	ICH_SGP38_PU
GPIO[39]	SDATAOUT0	I/O	Core	3.3V	GPI	ICH_SGP39_PU
GPIO[43:40]	OC[4:1]#	I/O	Resume	3.3V	Native	OC#0;OC#2;OC#4
GPIO[47:44]	OC[11:8]#	I/O	Resume	3.3V	Native	OC#6;OC#0
GPIO[48]	SDATAOUT1	I/O	Core	3.3V	GPI	ICH_SGP48_PU
GPIO[49]	unmuxed	I/O	Core	3.3V	GPO	DMI_STRAP
GPIO[50]	REQ1#	I/O	Core	5V	Native	PREQ1#
GPIO[51]	GNT1#	I/O	Core	3.3V	Native	PGNT1#
GPIO[52]	REQ2#	I/O	Core	5V	Native	PREQ2#
GPIO[53]	GNT2#	I/O	Core	3.3V	Native	PGNT2#
GPIO[54]	REQ3#	I/O	Core	5V	Native	PREQ3#
GPIO[55]	GNT3#	I/O	Core	3.3V	Native	PGNT3#
GPIO[56]	GLAN_DOCK#	I/O	Resume	3.3V	GPI	USB_DET2
GPIO[57]	CLGPIO5	I/O	Resume	3.3V	GPI	USB_DET3
GPIO[58]	SPI_CS1#	I/O	Resume	3.3V	GPI	SPI_CS1#
GPIO[59]	OC#0	I/O	Resume	3.3V	Native	OC#0
GPIO[60]	LINKALERT#	I/O	Resume	3.3V	Native	

SIO(W83667)

PIN NAME	USAGE	Input/Output	NOTES
GPIO11	BEEP	OUTPUT	BEEP sound output
GPIO12	HOOD_SW_DET#	INPUT	HOOD sense cable detect
GPIO13	CLEAR_PASSWORD	INPUT	Clear password detect
GPIO14	BOOT_BLOCK_RECOVERY	INPUT	BOOT BLOCK RECOVERY detect
GPIO15	BIZ_COVER	INPUT	BIZ COVER detect
GPIO16	SIO_SPI_WP#	OUTPUT	SPI ROM write protect
GPIO17	CPC_BPC_SW	INPUT	Chassis select detect
GPIO37	PWR_LED_SW	OUTPUT	POWER LED single / dual switch
GPIO50	5VDIMM_MODE	OUTPUT	Control USB_5V output for S3/S4/S5 states
GPIO70	MB_ID3	INPUT	MB_ID
GPIO71	MB_ID2	INPUT	MB_ID
GPIO72	MB_ID1	INPUT	MB_ID
GPIO73	MB_ID0	INPUT	MB_ID
GPIO76	SIO_ISOLATEB	OUTPUT	LAN chip isolate
GPIO53	LED_VSB	OUTPUT/OD	Power LED for VSB
GP46	GPIO_SYS_crash	OUTPUT/OD	Support after System PWR crash wake up

DDR-II DIMM Config.

DEVICE	ADDRESS	CLOCK	
DIMM 1	00	P/N_DDR0_A	P/N_DDR2_A
DIMM 2	01	P/N_DDR3_A	P/N_DDR5_A
DIMM 3	10	P/N_DDR0_B	P/N_DDR2_B
DIMM 4	11	P/N_DDR3_B	P/N_DDR4_B

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	CK_P_33M_S1

JUMPER SETTING

Clear CMOS(E50)	(1-2)NORMAL	(2-3)CLEAR

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Krishna (MS-7647)

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